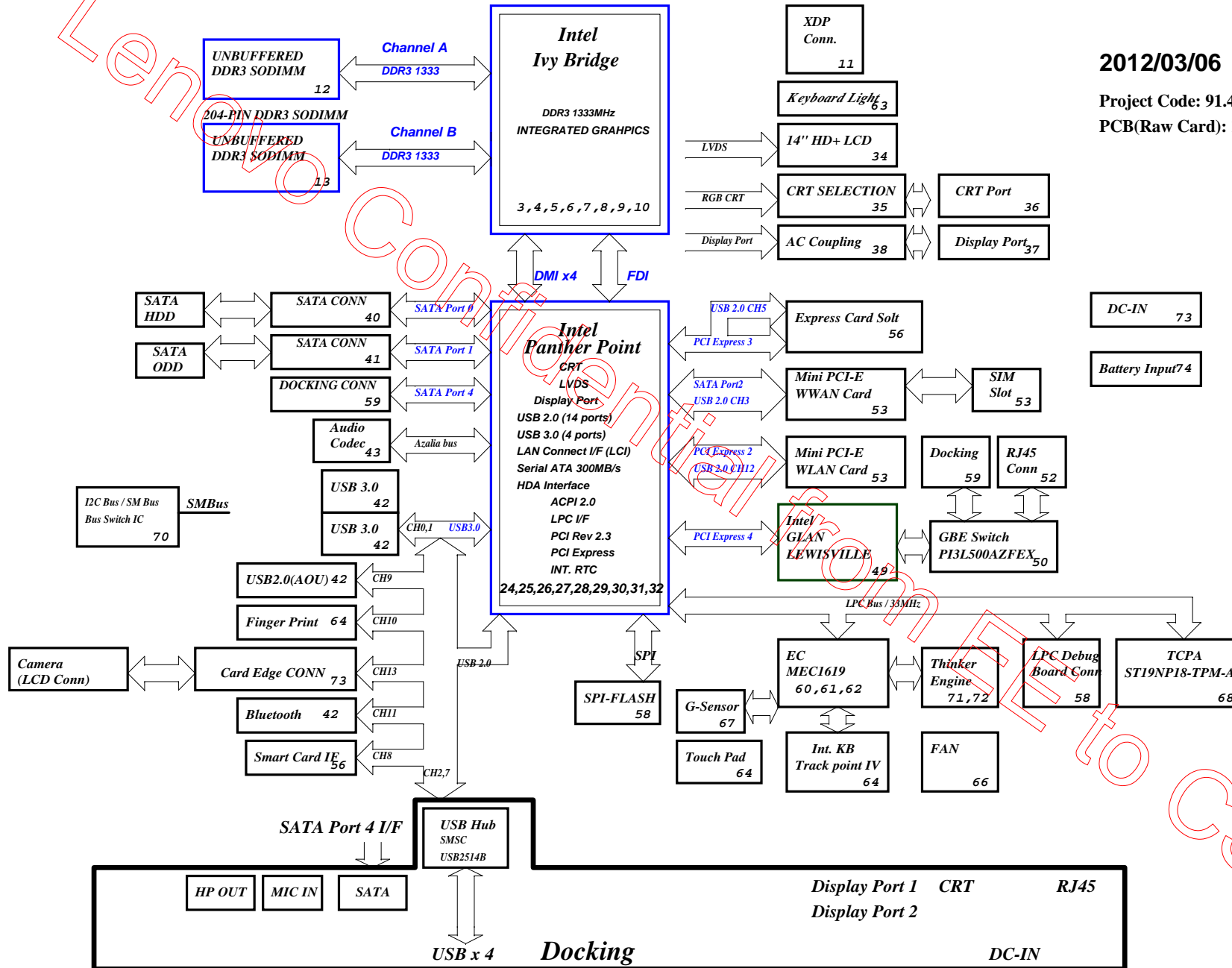


SHINAI-4 UMA Block Diagram

2012/03/06

Project Code: 91.4QZ01.001
PCB(Raw Card): 11263-1



PCB Layer Stackup

L1:TOP
L2:Signal 1
L3:GND
L4:Signal 2
L5:GND
L6:VCC
L7:Signal 3
L8:GND
L9:Signal4
L10:BOTTOM

Battery Charger/Selector

BQ24760 75
INPUTS OUTPUTS
DOCK_PWR20 CHARGER_OUT12

System DC/DC

TPS51220ARSN 79
VINT20 VCC5M
VCC3M

CPU DC/DC

VT1318M/VT1326S 80
VCC5M_OUT VCCCPUCORE

GMCH GFX CORE

VT1326S 81
VCC5M_OUT VCCGFXCORE

VCC1R5A

VT357FCX 86
VCC5M_OUT VCC1R5A

VCC0R75B

MAX1510 87
VCC1R5A VCC0R75B

VCC1R8B

BD9139 89
VCC5M_OUT VCC1R8B

VCC1R05AMT

VT356FCX 85
VCC5M_OUT VCC1R05LAN

VCC1R05B_VTT

VT356 84
VCC5M_OUT VCC1R05B_VTT

VCCSA

VT370 90
VCC5M_OUT VCCSA

Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.		
Block Diagram		
Title	Document Number	Rev
Size	Customer	Sheet
Date: Tuesday, March 06, 2012	Sheet	of 100

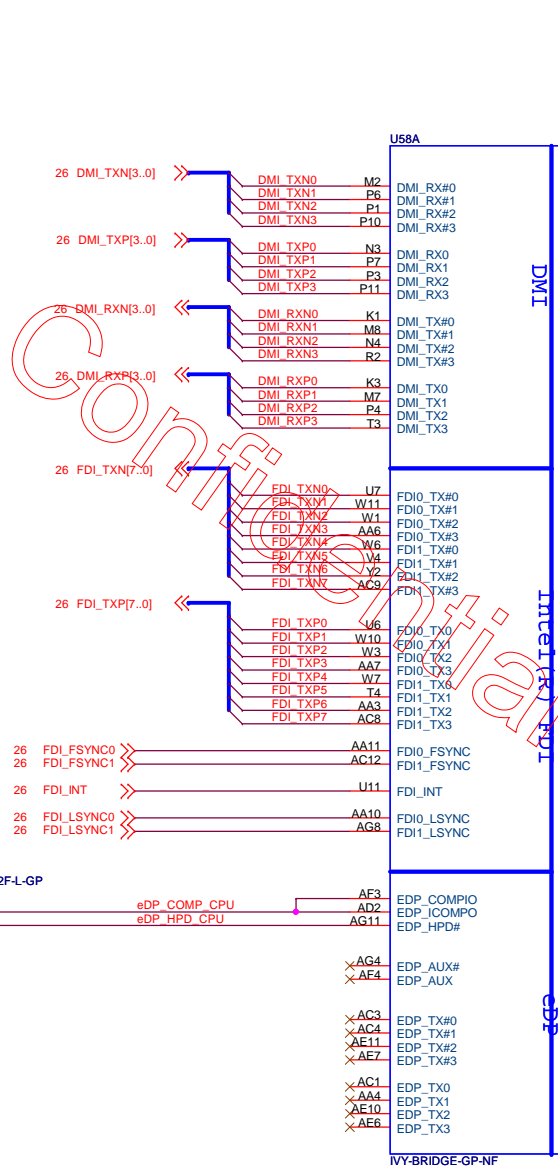
Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210

IBEXPEAK-M	39	38	48	49	Planar ID Version	Planar PCB Version
PLANAR_IDn	3	2	1	0		
	0	0	0	0	SHINAI-4 UMA initial	N/A
	0	0	0	1		
	0	0	1	0		
	0	0	1	1		
	0	1	0	0		
	0	1	0	1		
	0	1	1	0		
	0	1	1	1		
	1	0	0	0		
	1	0	0	1		
	1	0	1	0		

[illegible]

Lenovo



PCI EXPRESS -- GRAPHICS

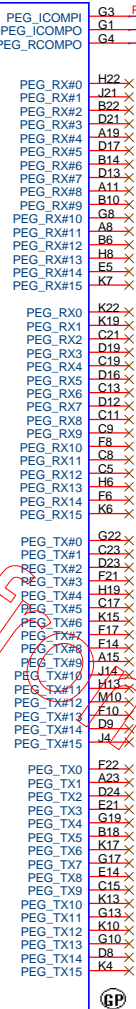
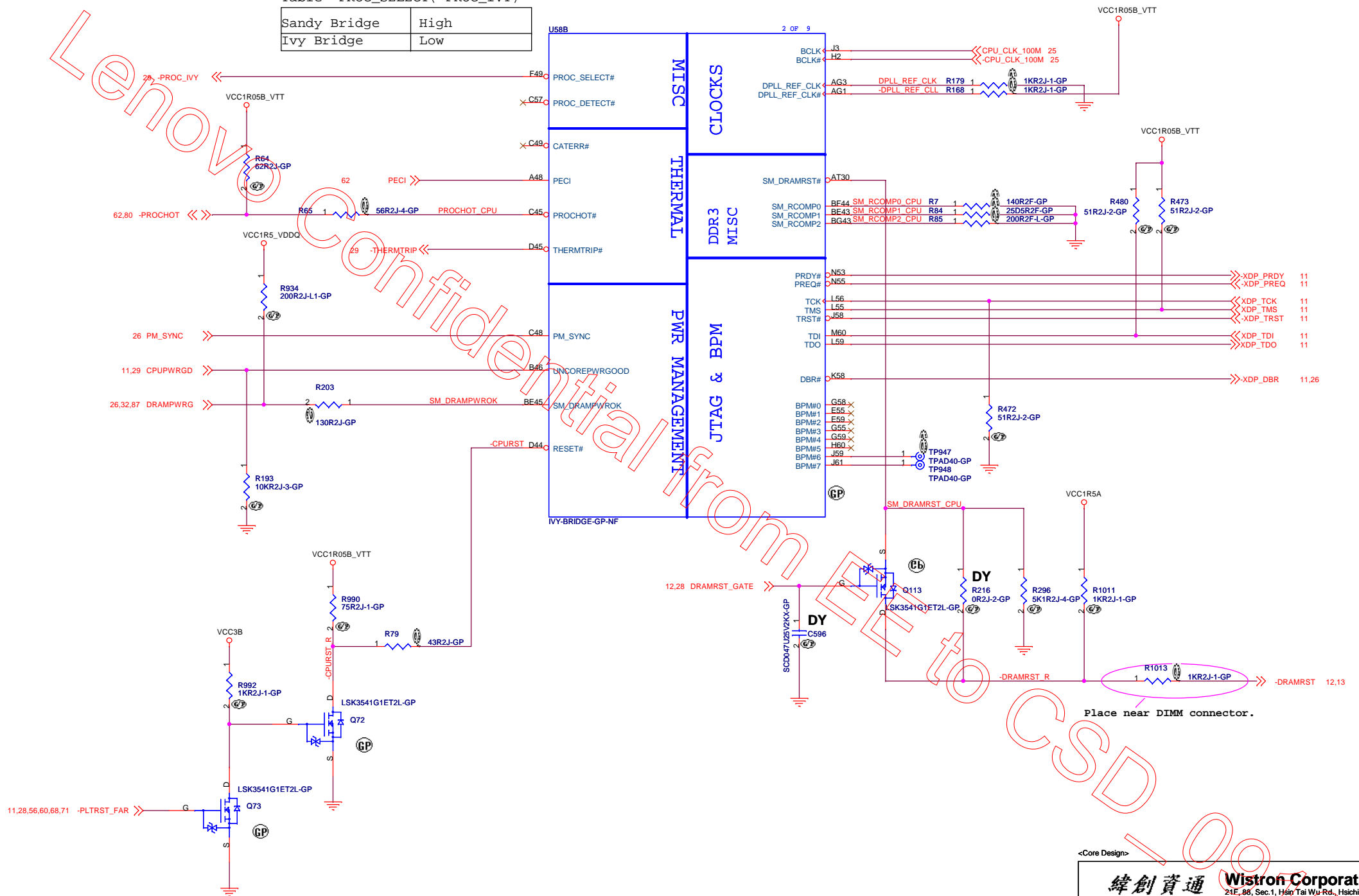


Table -PROC_SELECT(-PROC_IVY)

Sandy Bridge	High
Ivy Bridge	Low



<Core Design>

緯創資通

Wistron Corporation
21E, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 224, Taiwan, R.O.C.

Title CPU(2/8):CLK/MISC/JTAG

Size A3 Document Number

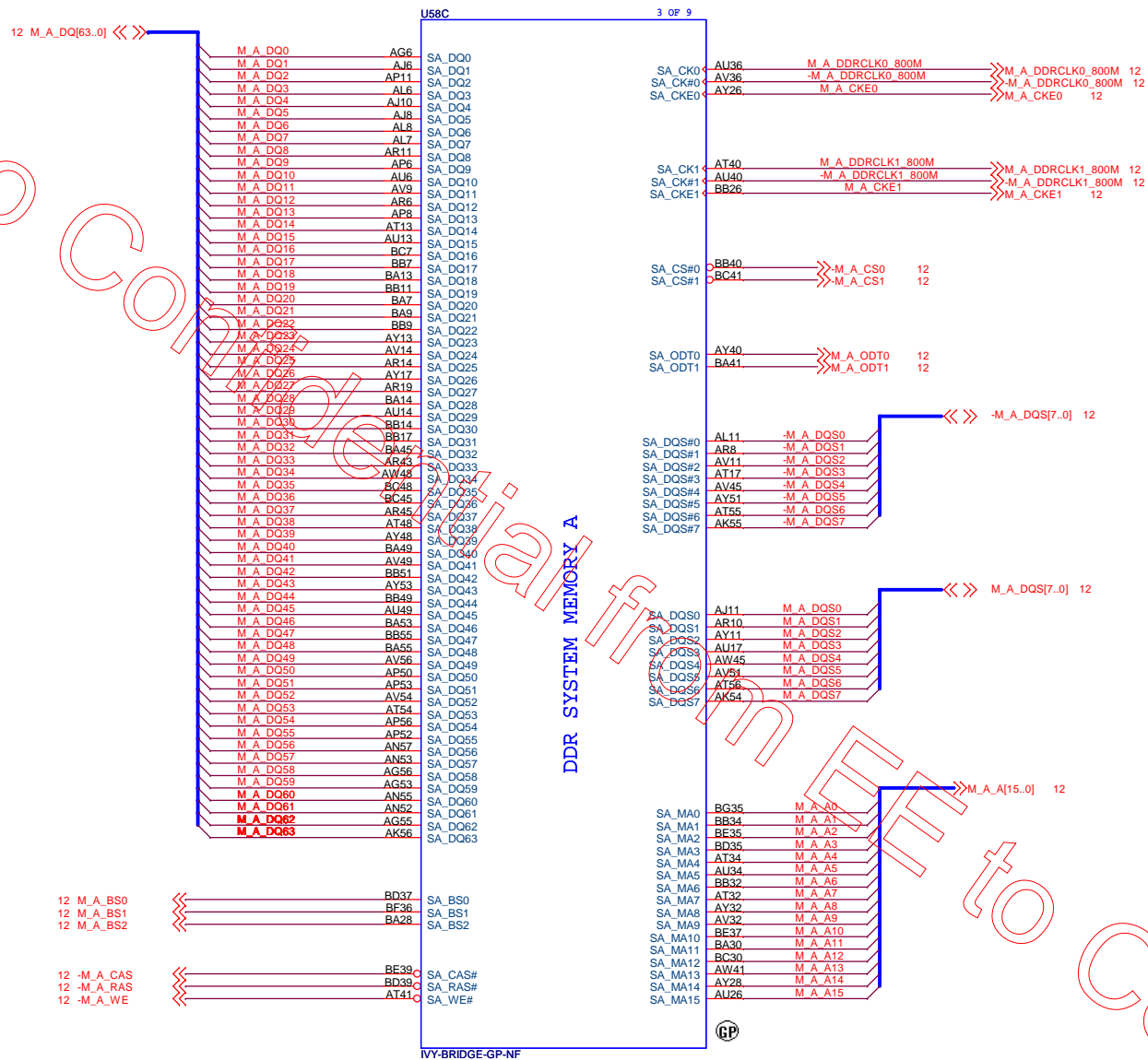
SHINAI-4 UMA

Rev -1

Date: Monday, March 12, 2012

Sheet 4 of 100

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緯創資通

Wistron Corporation
21E, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
CPU(3/8):DDR3 Channel-A

Size A3 Document Number SHINAI-4 UMA Rev -1

Date: Monday, March 12, 2012 Sheet 5 of 100

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DDR SYSTEM MEMORY B



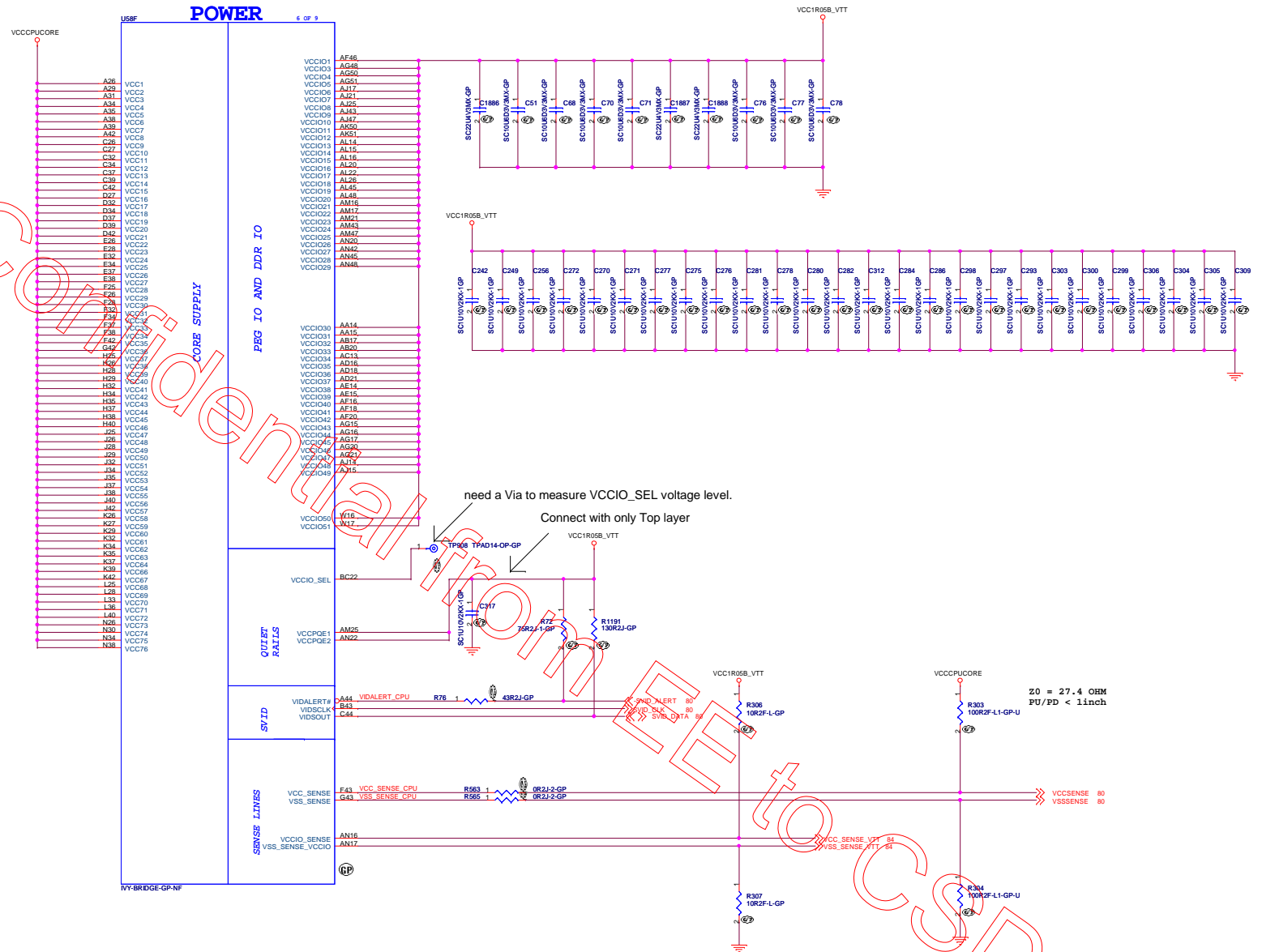
CSD

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緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title CPU(4/8):DDR3 Channel-B		
Size A3	Document Number SHINAI-4 UMA	Rev -1
Date: Monday, March 12, 2012 Sheet 6 of 100		

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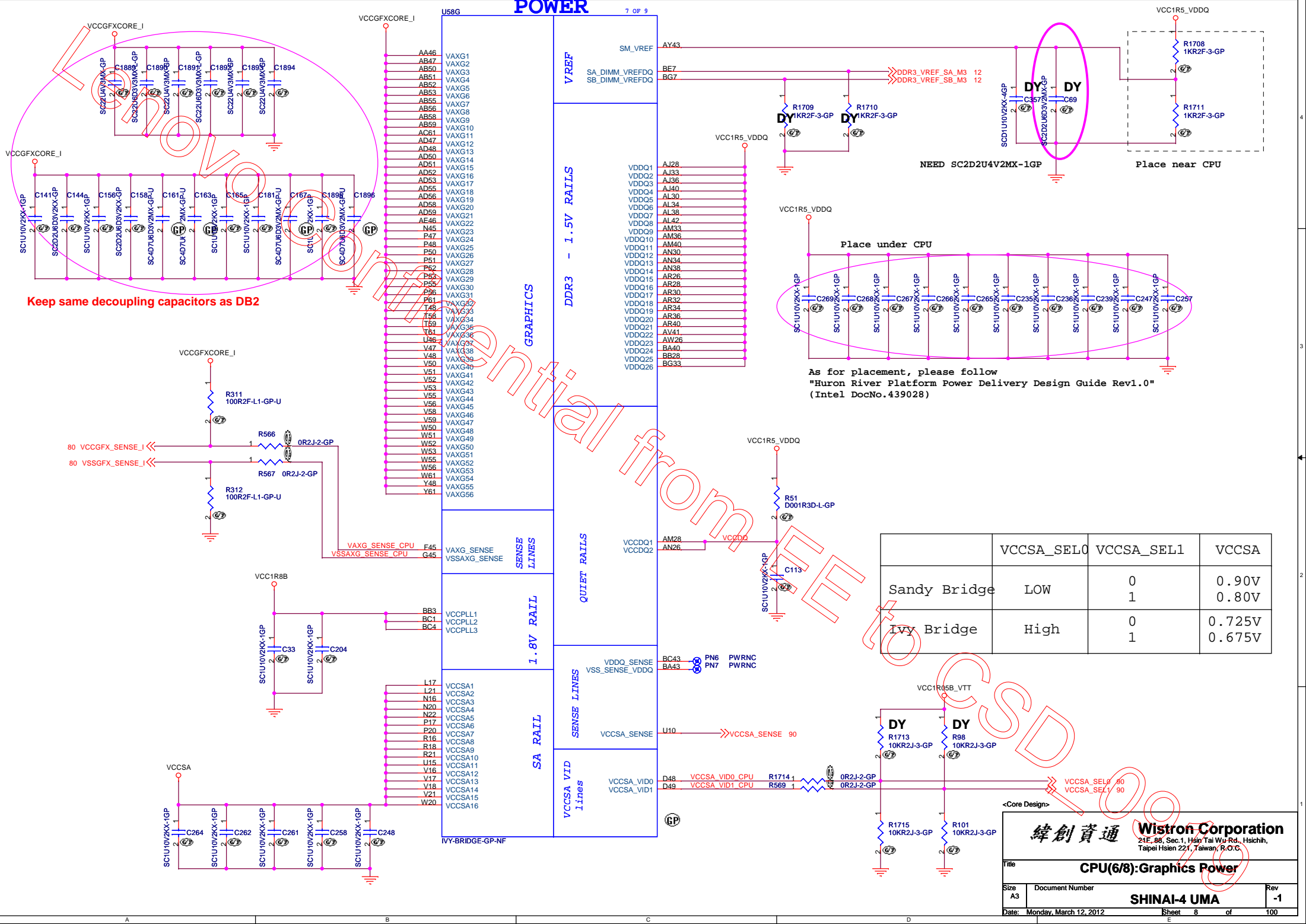
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&ltCore Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsien Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU(5/8):Processor Power
-------	---------------------------------

Size A2	Document Number SHINAI-4 UMA	Rev -1
Date: Monday, March 12, 2012 Sheet 7 of 100		



	VCCSA_SEL0	VCCSA_SEL1	VCCSA
Sandy Bridge	LOW	0 1	0.90V 0.80V
Ivy Bridge	High	0 1	0.725V 0.675V

緯創資通

Wistron Corporation

21E, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU(6/8):Graphics Power

Size

A3

Document Number

SHINAI-4 UMA

Date

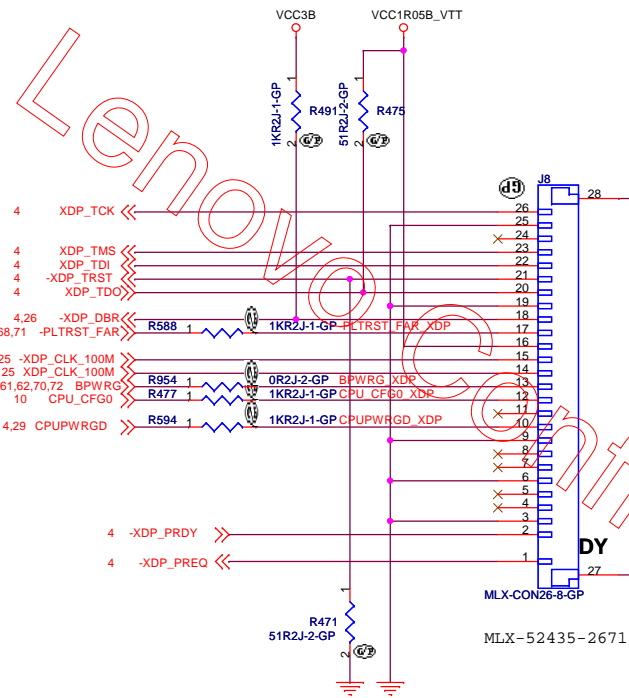
Monday, March 12, 2012

Sheet

8 of 100

Rev

-1

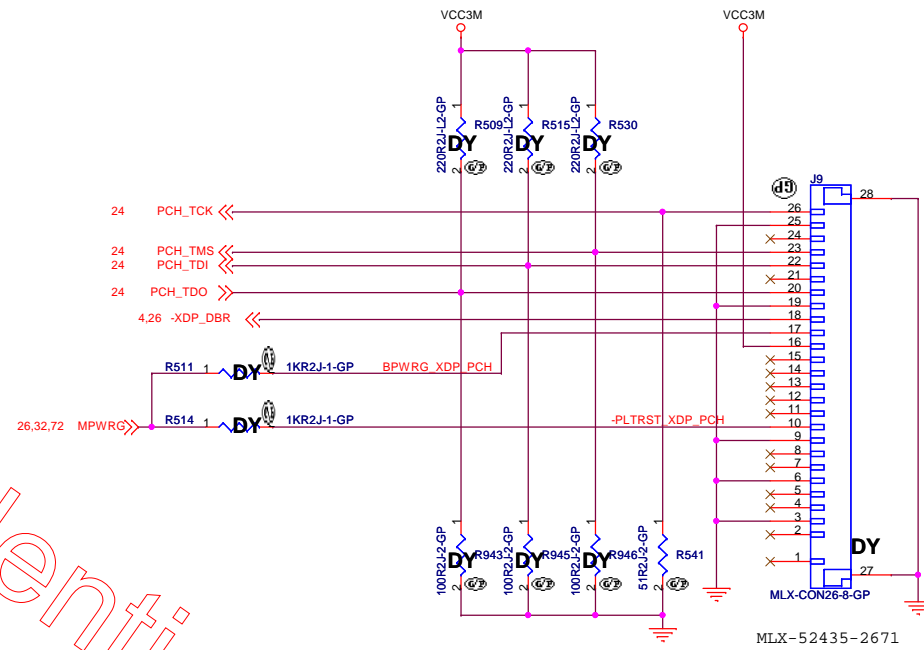


DEBUG Interface for Processor.

XDP1

		ENABLE	DISABLE
TDO	R45	ASM	DY
TRST#	R59	ASM	ASM
DBRST#	R44	ASM	ASM
RESET#	R49	ASM	DY
CFG0	R51	ASM	DY
PWRGD	R53	ASM	DY
BPWRG	R50	ASM	DY
	CN24	ASM	DY

SDV Logic



DEBUG Interface for PCH.

XDP2

		ENABLE	DISABLE
TDO	R46	220	DY
	R55	100	DY
TMS	R48	220	DY
	R57	100	DY
TDI	R47	220	DY
	R56	100	DY
TCK	R58	51	51
MPWRG	R52	ASM	DY
	R54	ASM	DY
	CN25	ASM	DY

Logic

<Core Design>

緯創資通 Wistron Corporation
21E, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			XDP Connector	
Size	Document Number	SHINAI-4 UMA		Rev
A3				-1
Date:	Monday, March 12, 2012	Sheet	11	of 100

Lenovo

Place caps near Slot-A (J21) pin 126

Place caps near Slot-A (J21) pin 1 as possible

5 M_A_A[15..0]

5 M_A_BS2

5 M_A_BS0

5 M_A_BS1

5 M_A_DQ[63..0]

5 M_A_DQS[7..0]

5 M_A_DQS[7..0]

5 M_A_ODT0

5 M_A_ODT1

DDR3_VREF_CA

DDR3_VREF_DQ_SA

DDR3_VREF_DQ_SB

DDR3_VREF_SA_M3

DDR3_VREF_SB_M3

DDR3_VREF_CA

DDR3_VREF_DQ_SA

DDR3_VREF_DQ_SB

DDR3_VREF_SA_M3

DDR3_VREF_SB_M3

DDR3_VREF_CA

DDR3_VREF_DQ_SA

DDR3_VREF_DQ_SB

DDR3_VREF_SA_M3

DDR3_VREF_SB_M3

DDR3_VREF_CA

DDR3_VREF_DQ_SA

DDR3_VREF_DQ_SB

DDR3_VREF_SA_M3

DDR3_VREF_SB_M3

REVERSE TYPE

Place one cap to each power pin and as close as possible

VCC1R5A

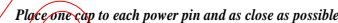
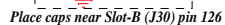
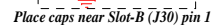
VCC0R75B

DDR3-204P-143-GP-U1
SKT DDR3 204P 2-1932823-1 SMD

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緯創資通 Wistron Corporation
21F, 8F, Sec. 1, Hsin Tai Wu Rd., Hsinchu,
Taipei Hsien 301, Taiwan, R.O.C.

Title		DDR3 SODIMM-A
Size	Document Number	SHINAI-4 UMA
A2		Rev -1
Date: Monday, March 12, 2012	Sheet 12	of 100



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Taipei Hsien 221, Taiwan, R.O.C.

Title

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Size

A3

Document Number

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Rev

-1

Date: Tuesday, March 06, 2012

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Date: Tuesday, March 06, 2012		Sheet 15 of	100

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Date: Monday, September 17, 2012		Sheet 17 of 100

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Title

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Date: Tuesday, March 06, 2012		Sheet 23 of	100

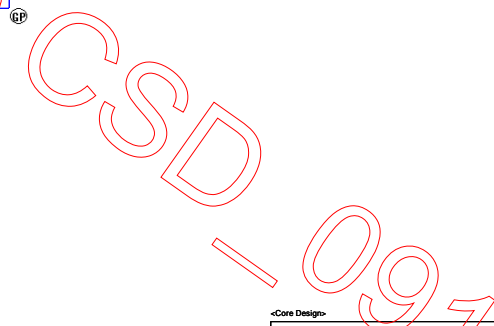
CONFIDENTIAL

DO NOT CHANGE THESE PARTS

43 HDA_BCLK <<
 43 HDA_SYNC <<
 DETECT 28
 48 PCH_SMB >>
 43 -HDA_RST >>
 43 HDA_SIN0 >>
 43 HDA_SDO <<

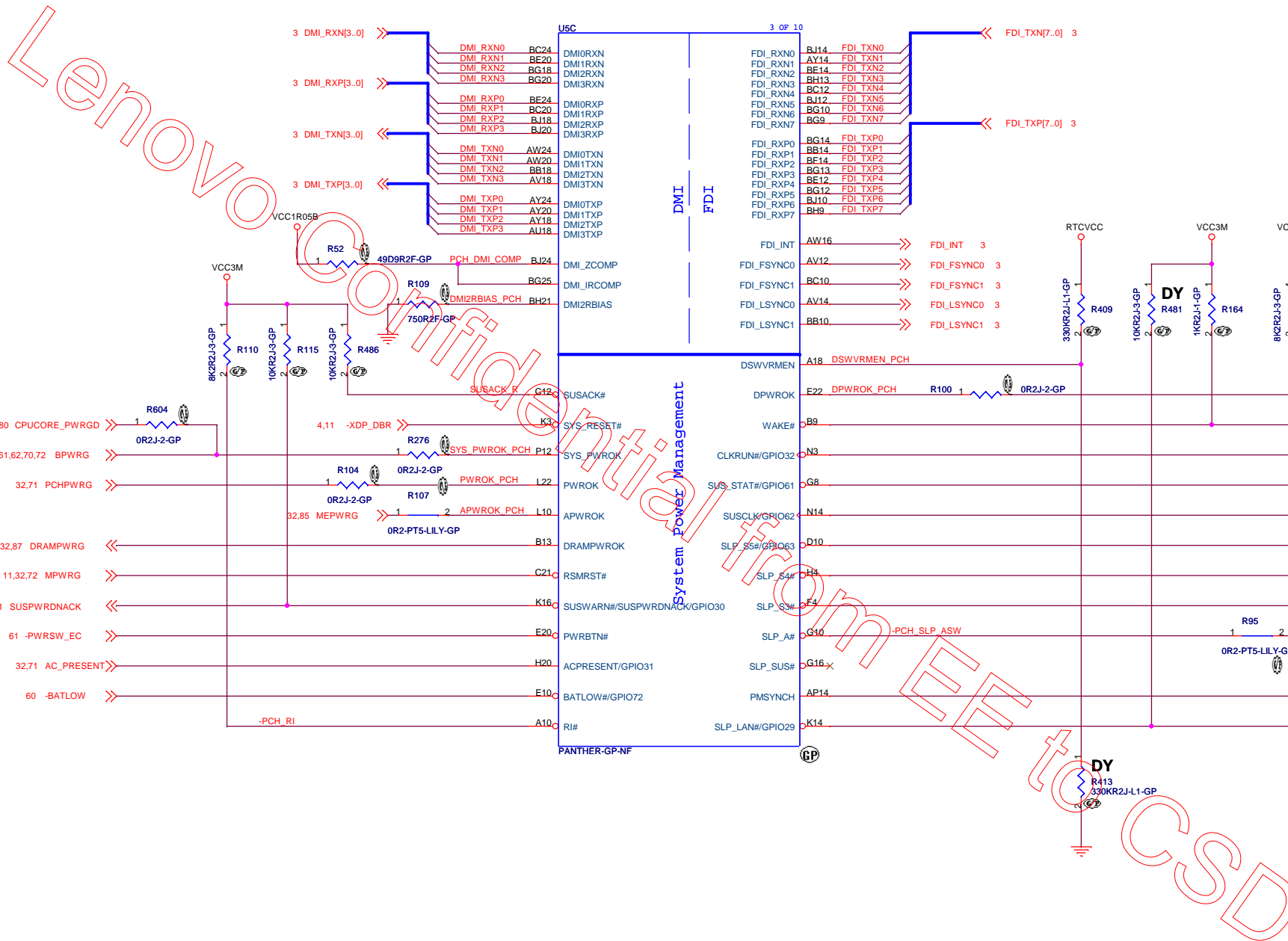
Place on Top side

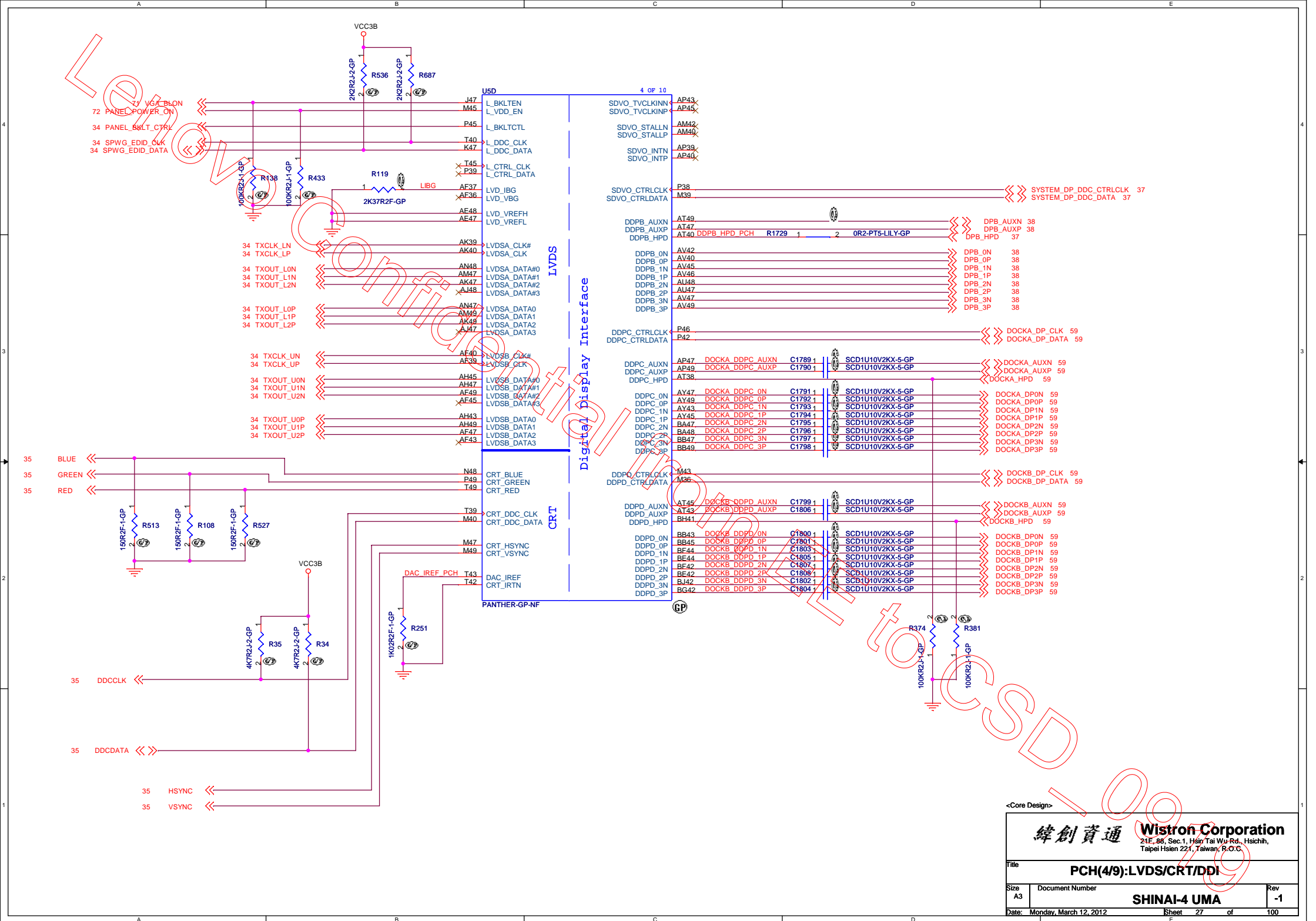
Place on TOP side
 Do NOT move after fix

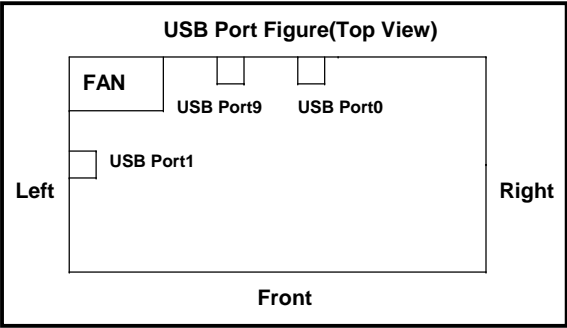
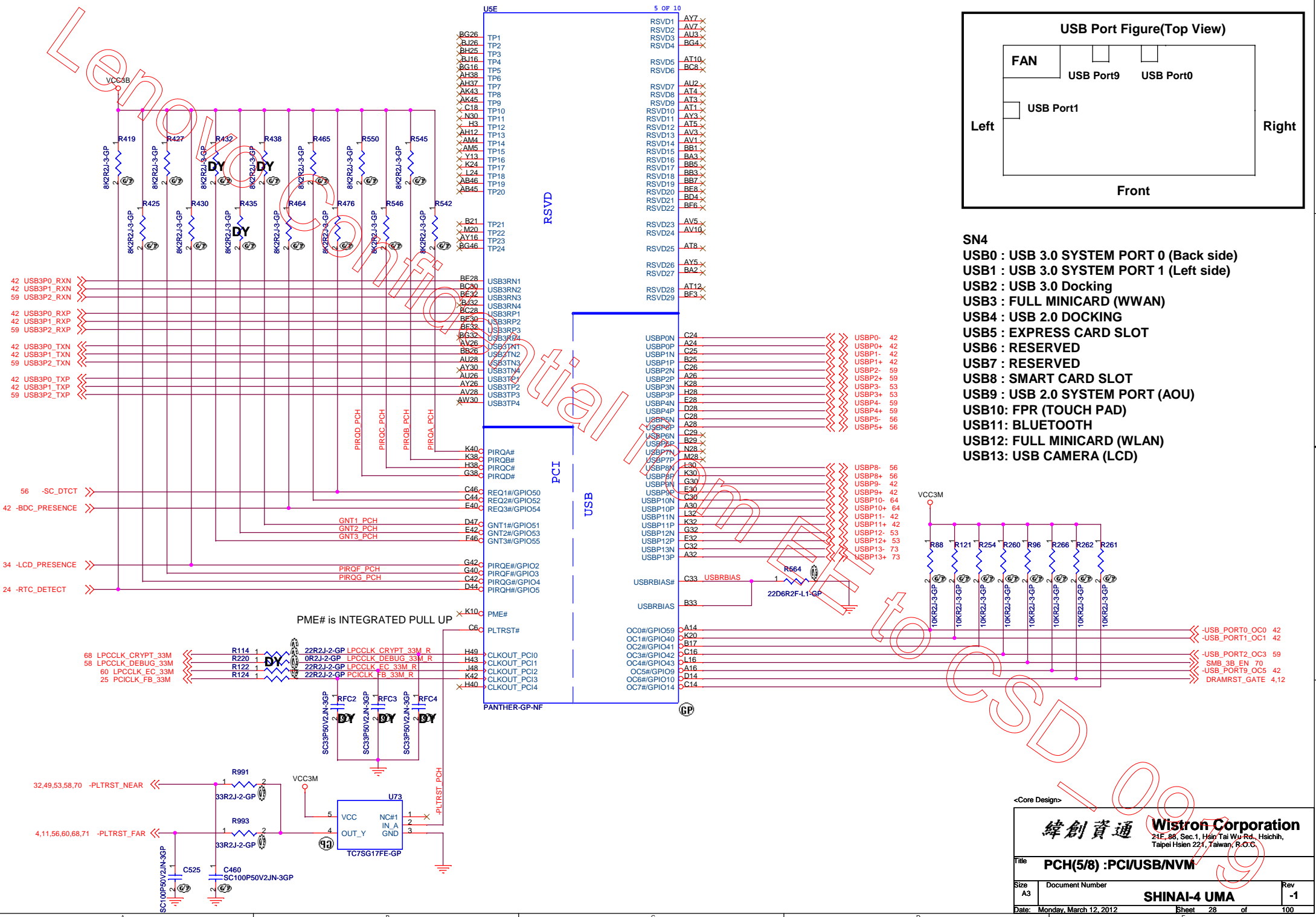


LOGIC

SPKR	TCO TIMER SYSTEM REBOOT
HIGH	DISABLED(NO REBOOT)
LOW	ENABLED



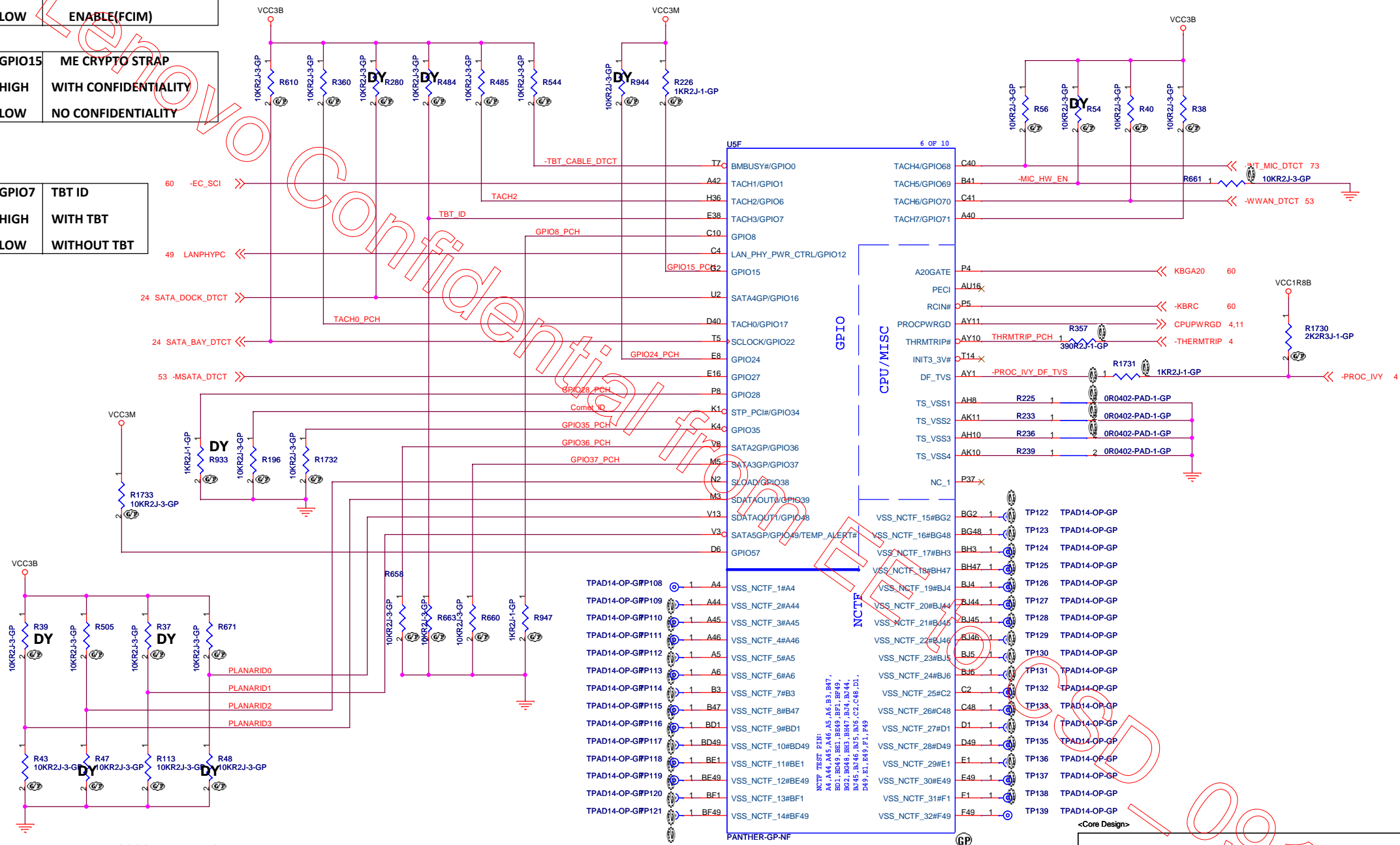




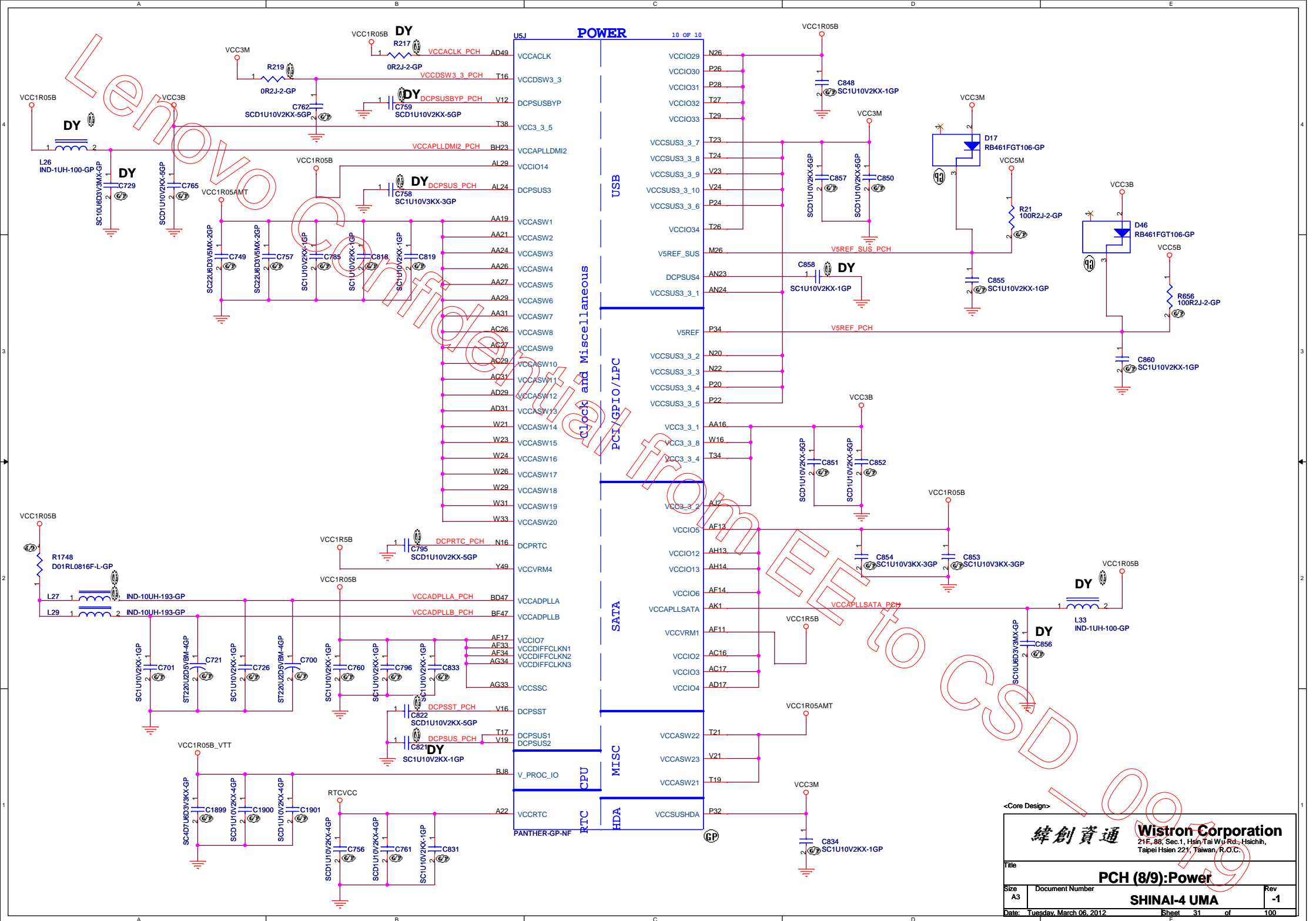
- SN4
- USB0 : USB 3.0 SYSTEM PORT 0 (Back side)
 - USB1 : USB 3.0 SYSTEM PORT 1 (Left side)
 - USB2 : USB 3.0 Docking
 - USB3 : FULL MINICARD (WWAN)
 - USB4 : USB 2.0 DOCKING
 - USB5 : EXPRESS CARD SLOT
 - USB6 : RESERVED
 - USB7 : RESERVED
 - USB8 : SMART CARD SLOT
 - USB9 : USB 2.0 SYSTEM PORT (AOU)
 - USB10: FPR (TOUCH PAD)
 - USB11: BLUETOOTH
 - USB12: FULL MINICARD (WLAN)
 - USB13: USB CAMERA (LCD)

GPIO15	ME CRYPTO STRAP
HIGH	WITH CONFIDENTIALITY
LOW	NO CONFIDENTIALITY

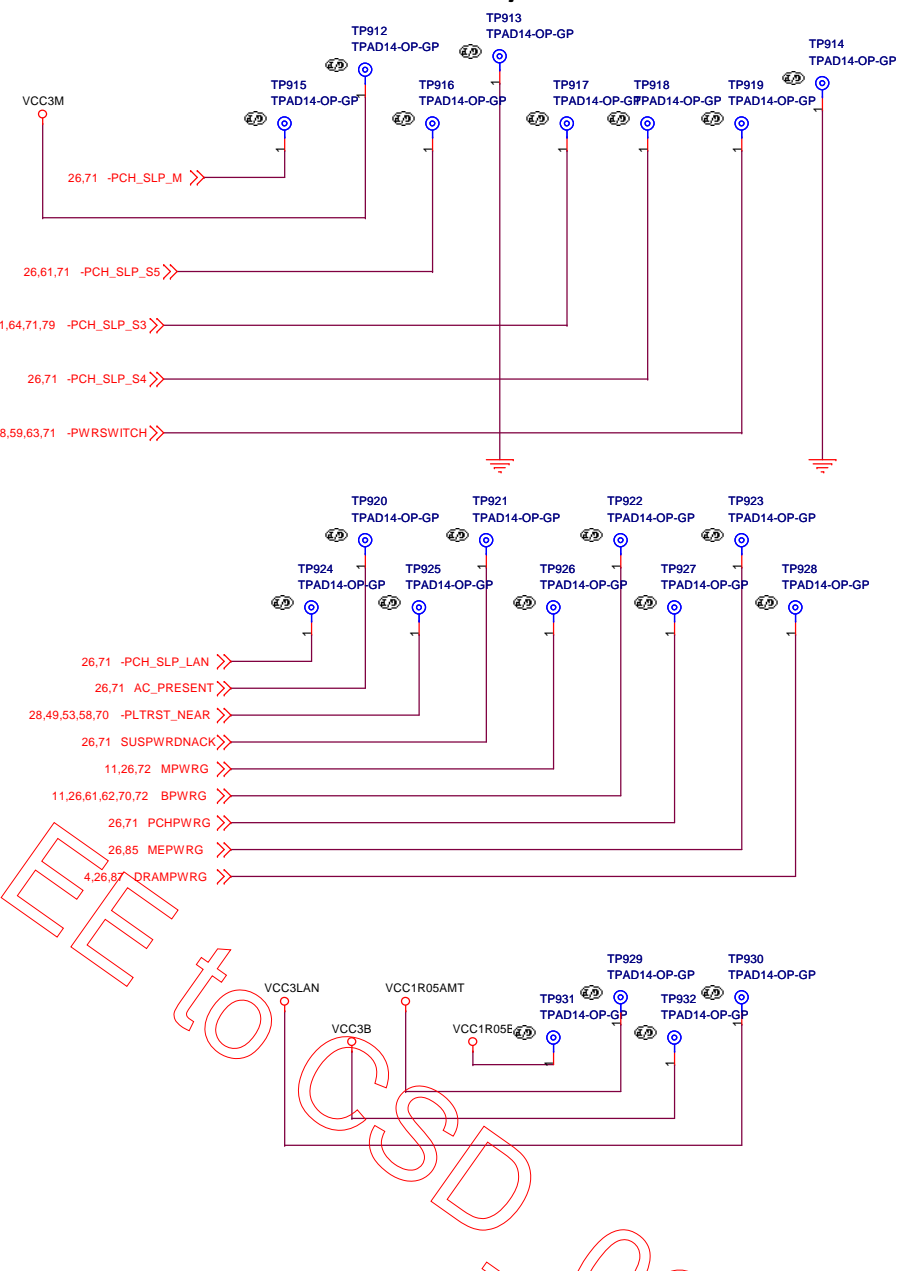
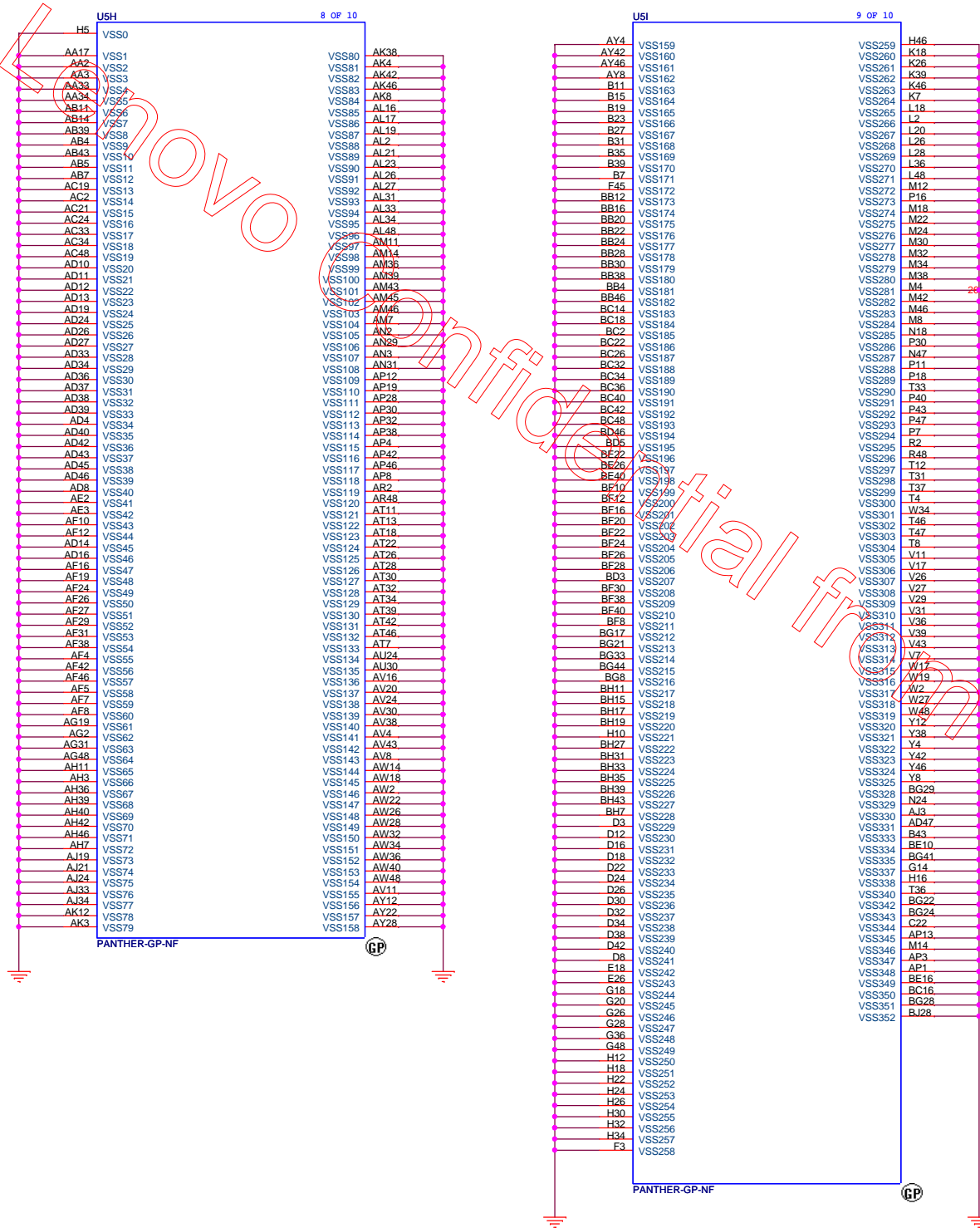
GPIO7	TBT ID
HIGH	WITH TBT
LOW	WITHOUT TBT



PLANAR ID: 0000	UMA w/o TBT SDV
0001	TBT & SWG SDV
0010	UMA & SWG FVT
0011	UMA & SWG SIT
0100	UMA & SWG SIT-R
0101	UMA & SWG SVT



TEST PAD FOR METS/APS



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (9/9):GND**

Size: A3 Document Number: **SHINAI-4 UMA** Rev: **-1**

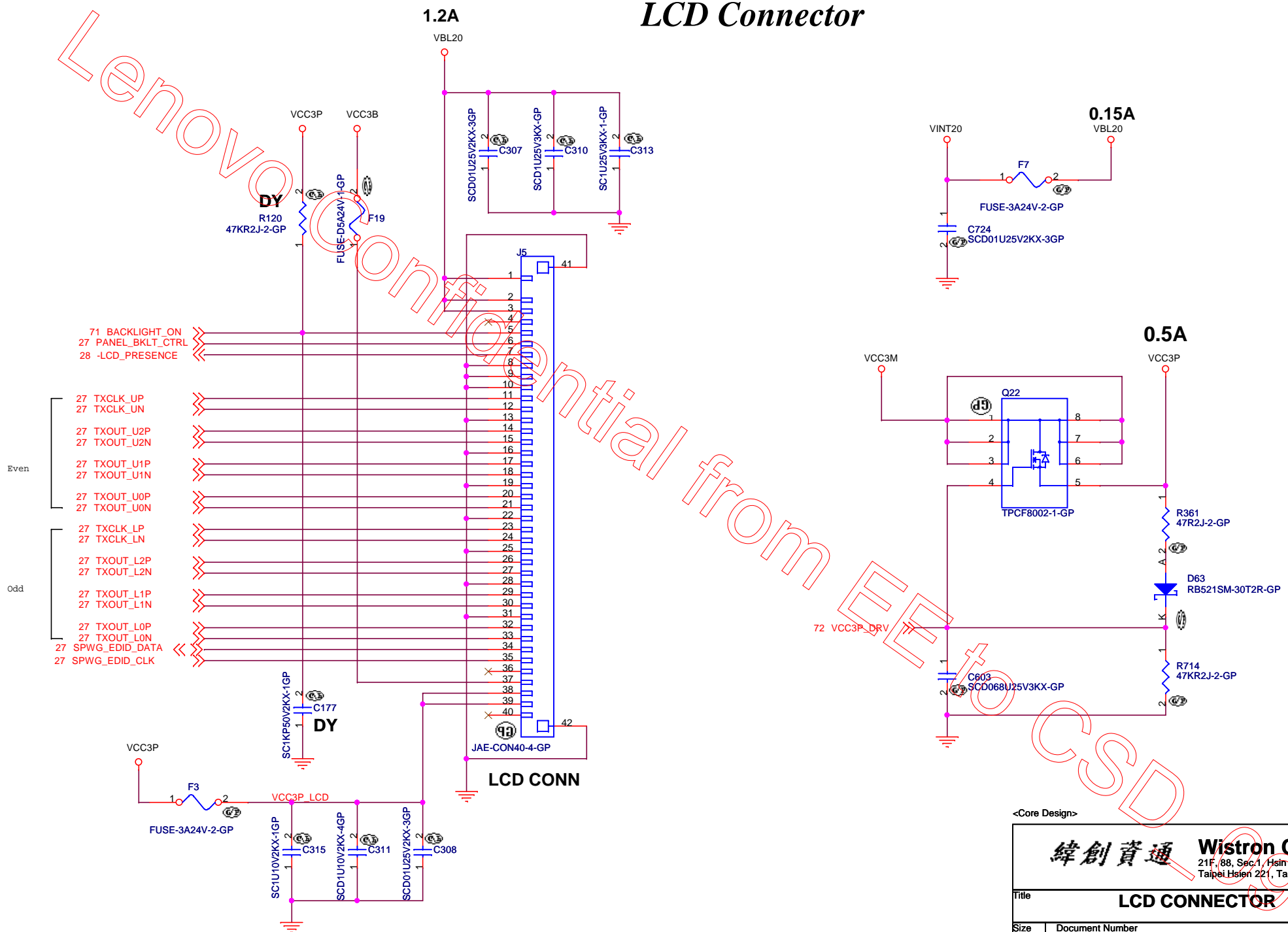
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Title			
LPM LVDS SW/Connector			
Size	Document Number		Rev
A3	SHINAI-4 UMA		-1
Date:	Tuesday, March 06, 2012	Sheet	33 of 100

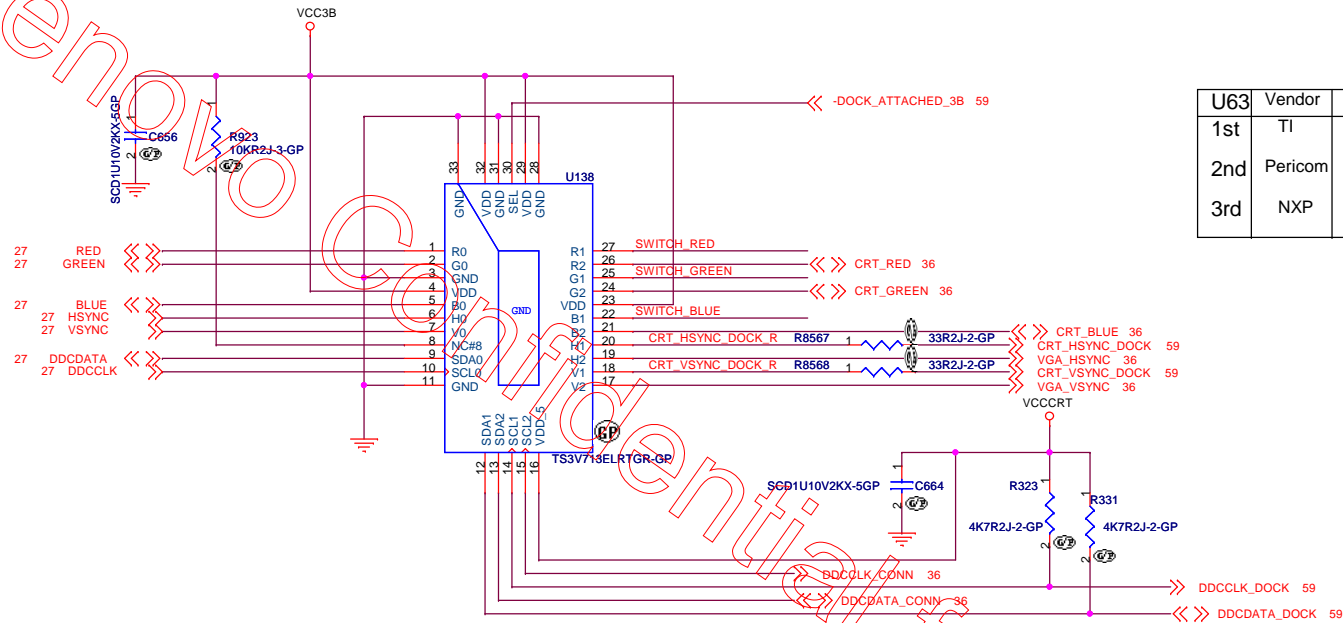
LCD Connector



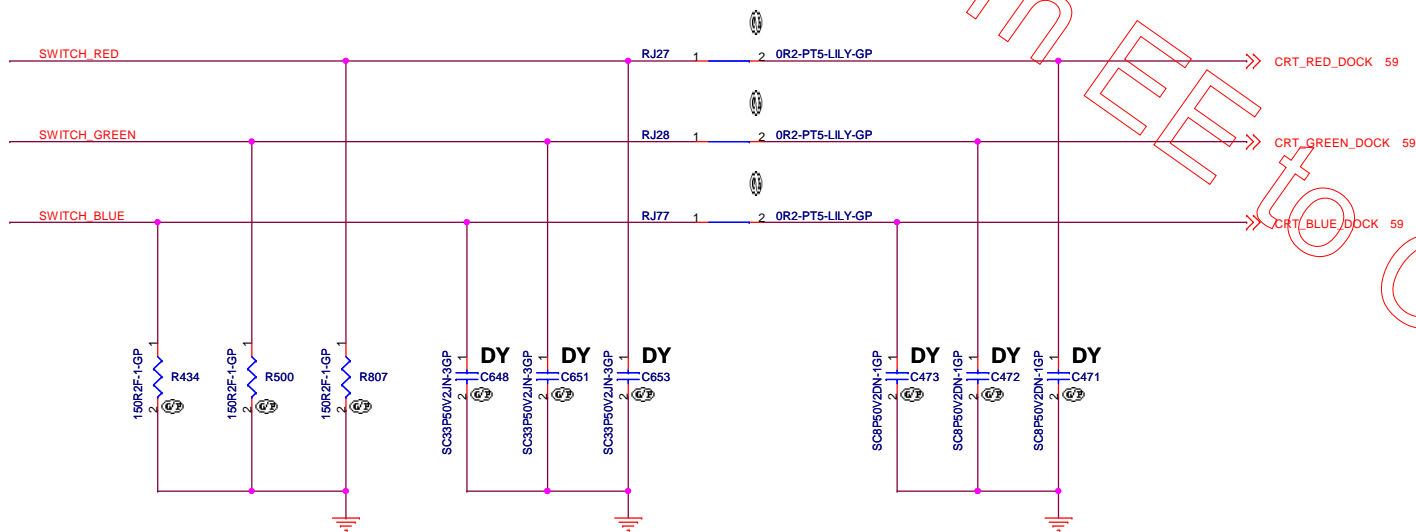
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緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
LCD CONNECTOR			
Size	Document Number	Rev	
Custom	SHINAI-4 UMA	-1	
Date:	Monday, March 12, 2012	Sheet	34 of 100

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U63	Vendor	Vendor P/N	Wistron P/N
1st	TI	TS3V713EL	73.03713.003
2nd	Pericom	PI3V713	73.3V713.00I
3rd	NXP	NX5DV715HF	73.05715.003



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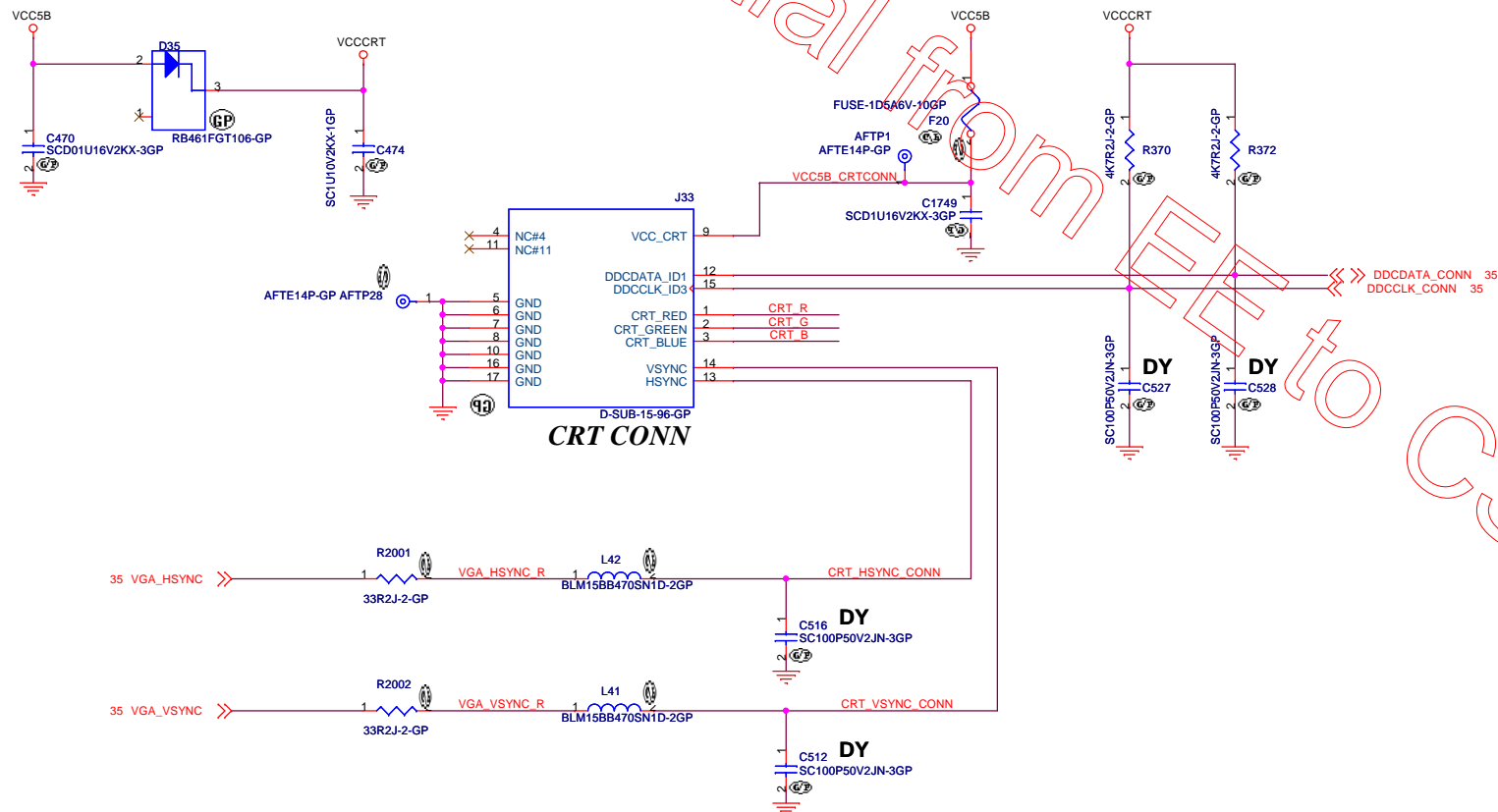
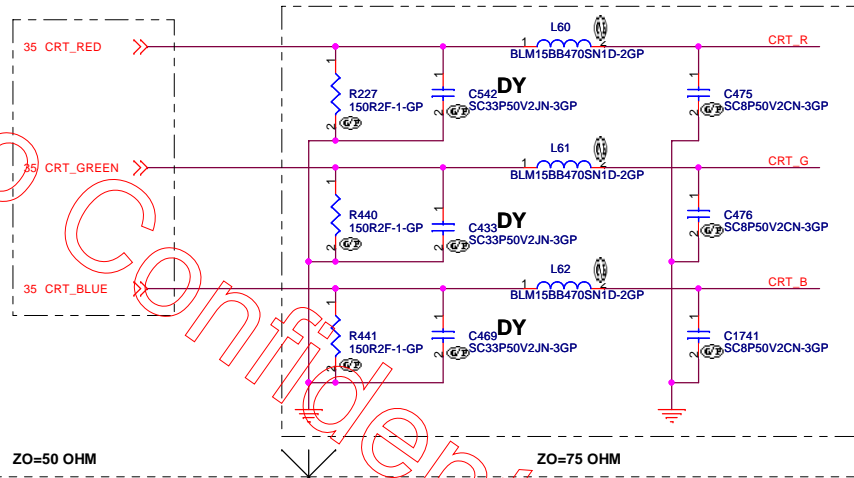
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Title			
CRT SELECTOR			
Size A3	Document Number SHINAI-4 UMA		Rev -1
Date: Monday, March 12, 2012	Sheet	35 of	100

GND GUARDING

EACH SIGNAL WIDTH DEPENDS ON ZO(TRACE IMPEDANCE)

SPACING=20MIL

Near CRT Connector



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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
Ext CRT Interface			
Size A3	Document Number	SHINAI-4 UMA	
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System DP Connector



<Core Design>

緯創資通			Wistron Corporation		
			21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
Display Port AC Coupling					
Size	Document Number				Rev
A4	SHINAI-4 UMA				-1
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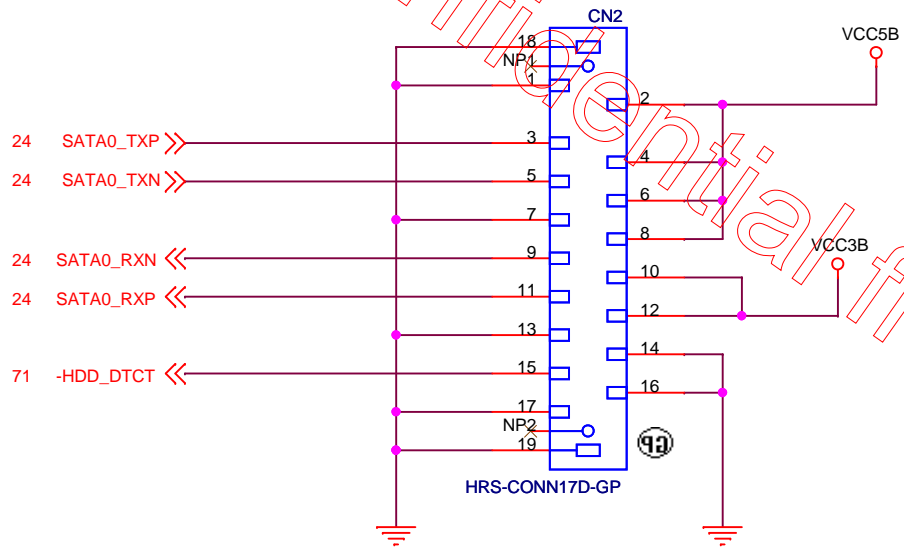
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A4	SHINAI-4 UMA				-1
Date: Tuesday, March 06, 2012		Sheet 39		of 100	

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Title

SATA HDD Connector

Size
A4

Document Number

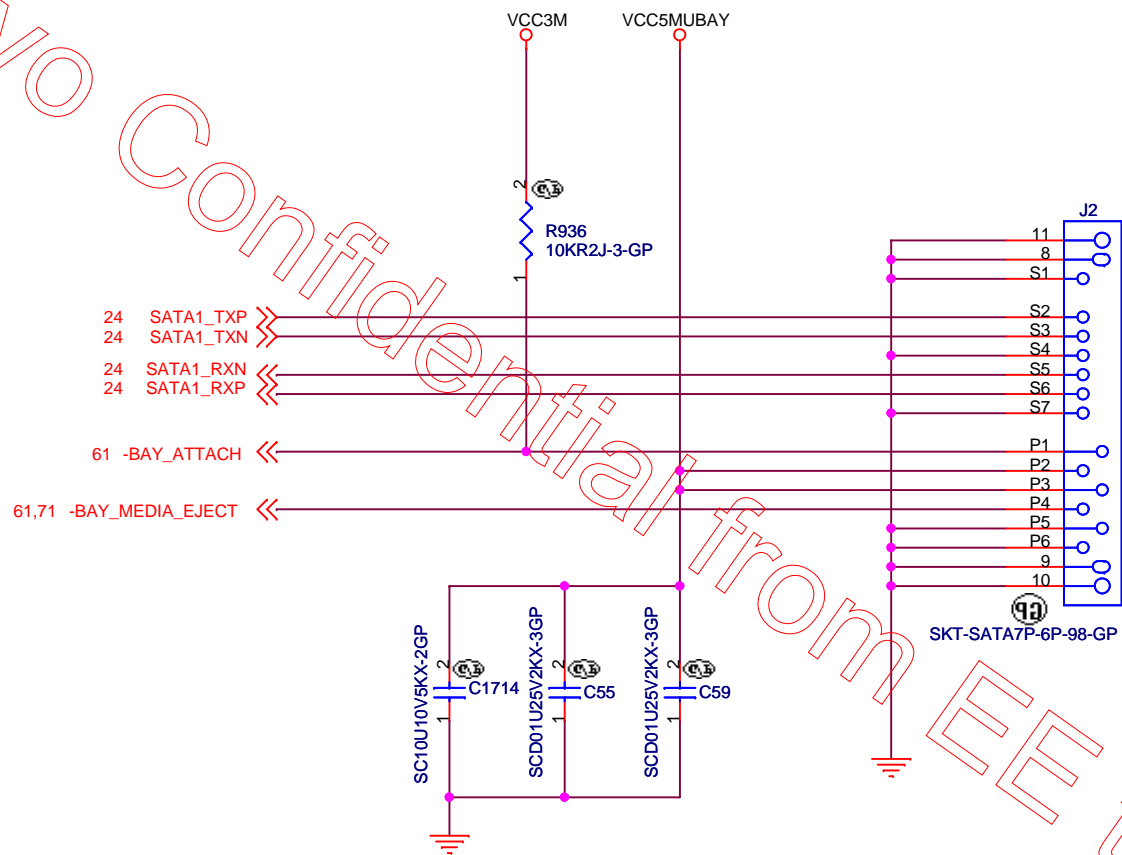
SHINAI-4 UMA

Rev
-1

Date: Monday, March 12, 2012

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緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

SATA ODD BAY

Size
A4

Document Number

SHINAI-4 UMA

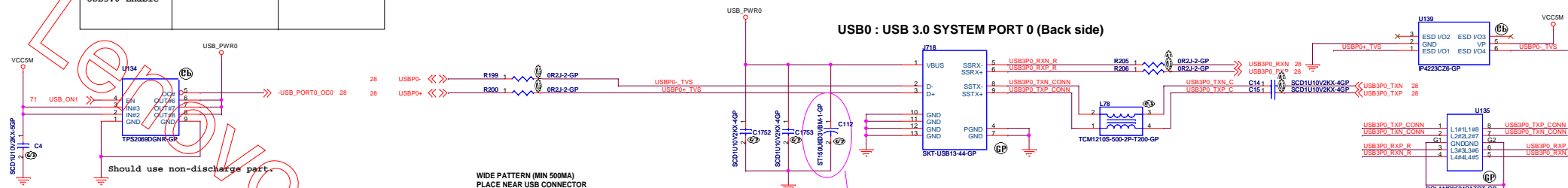
Rev
-1

Date: Monday, March 12, 2012

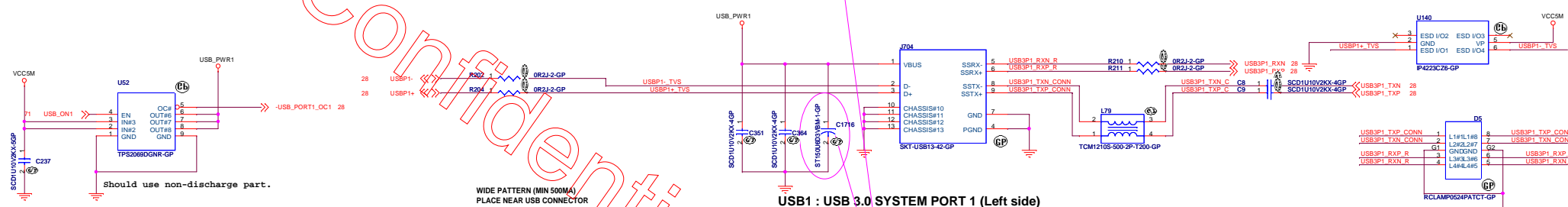
Sheet 41 of 100

USB3.0 port0

U52,U134		
USB3.0 Enable	TI TPS2069DGN GMT G548A1F51U	74.02069.079 74.00548.A79

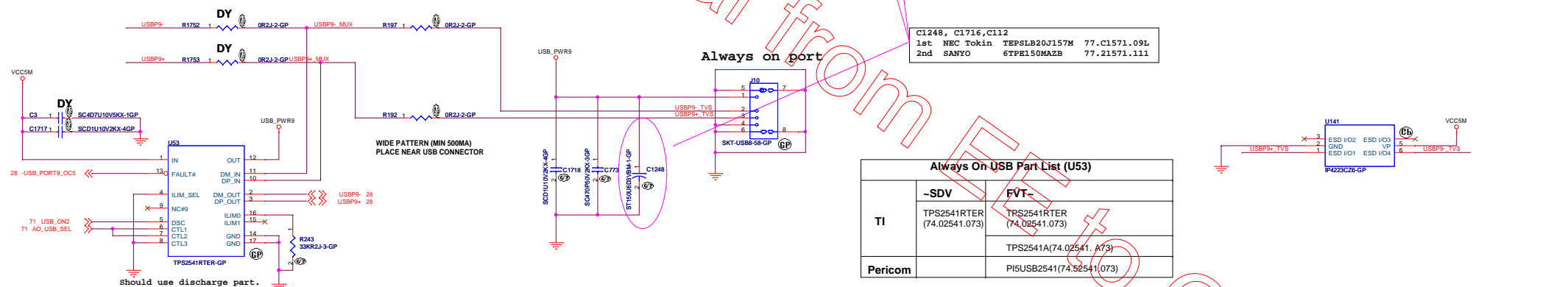


USB3.0 port1

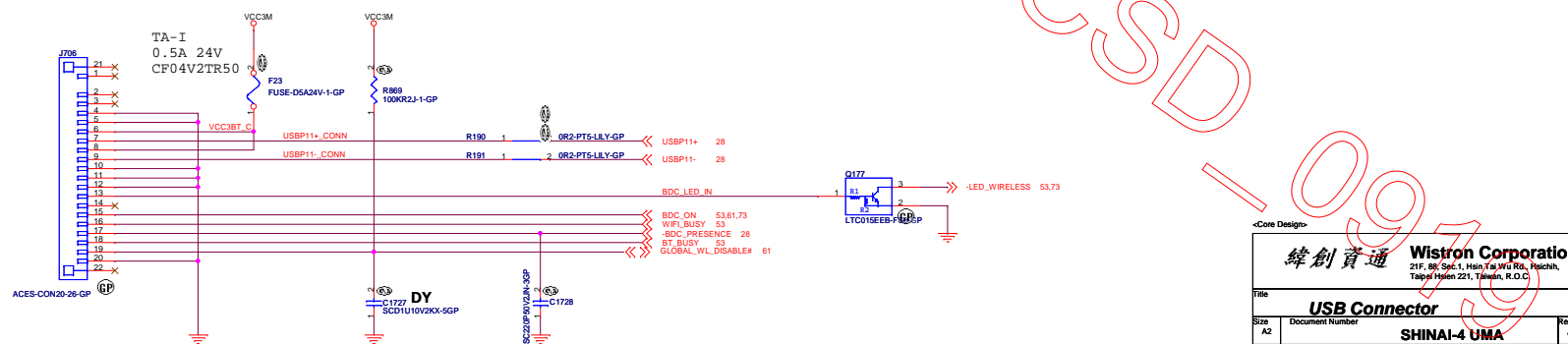


USB port9(Always On USB)

Dual Layout



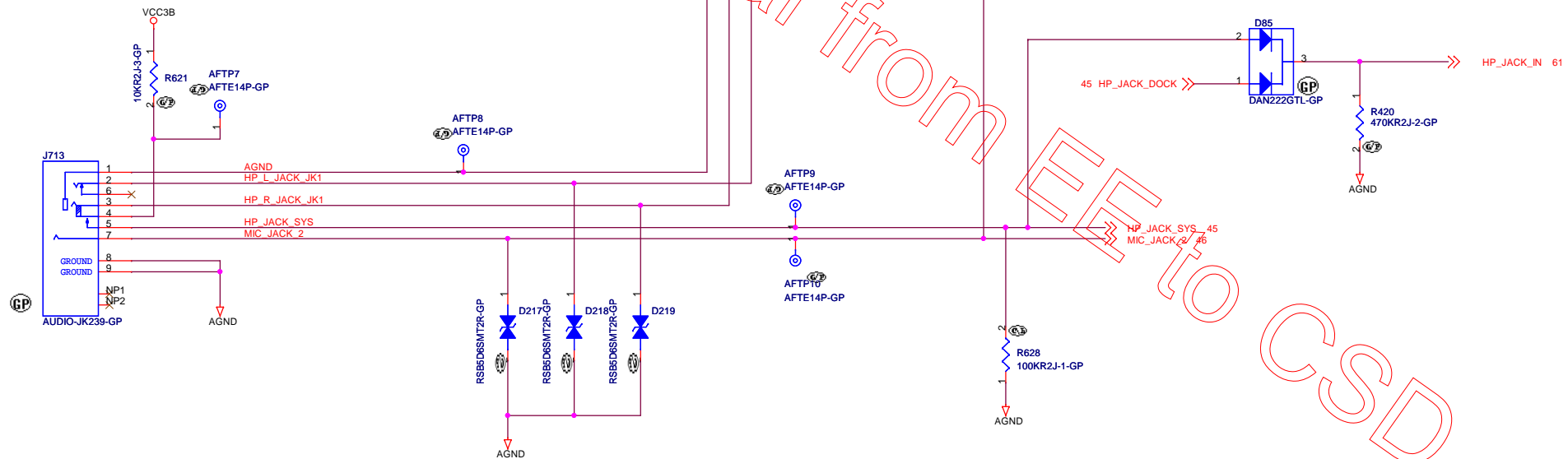
Bluetooth Module & WIRELESS DISABLE SW



NEAR HEADPHONE CONN

WIDE PATTERN

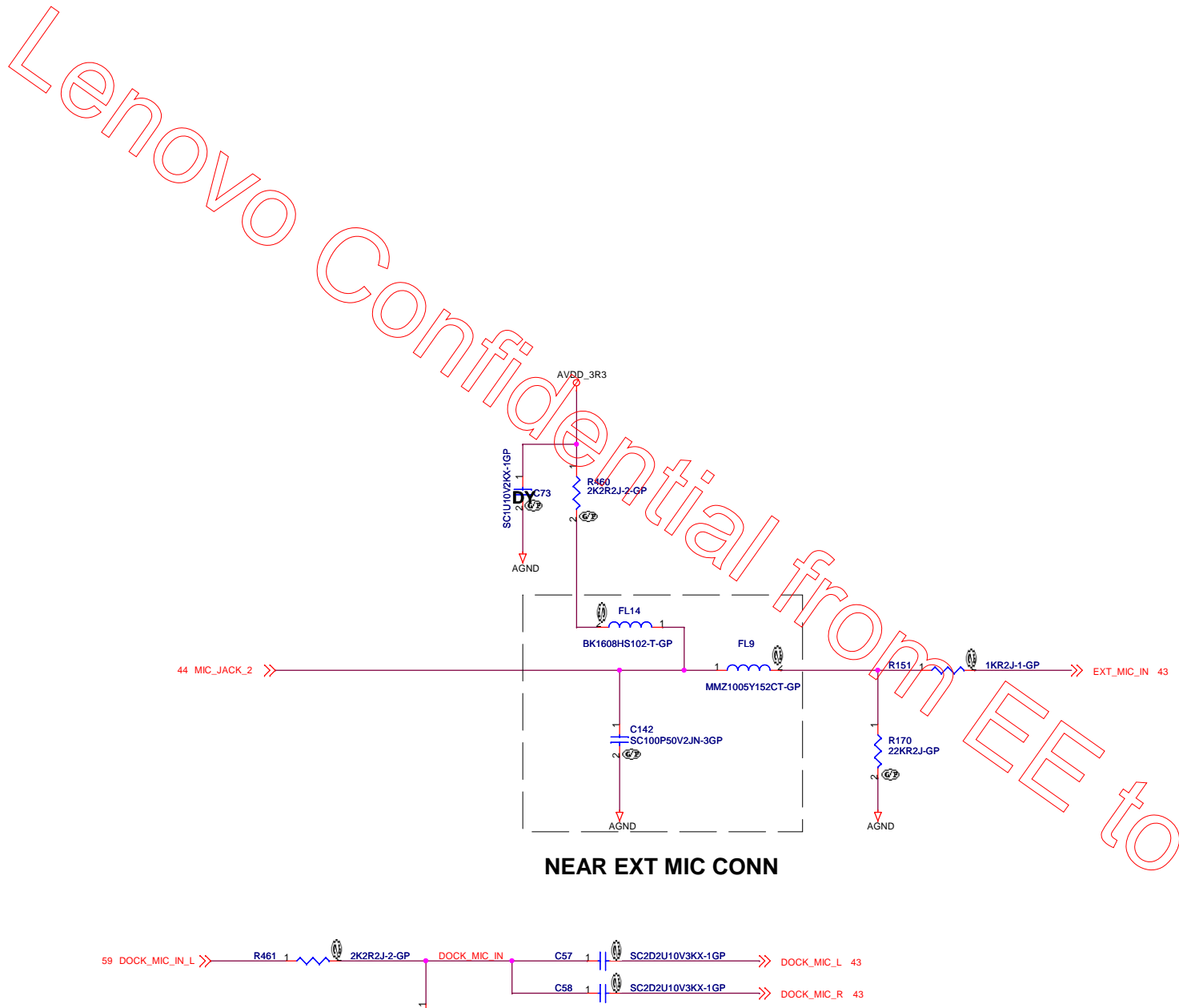
WIDE AND SHORT PATTERN



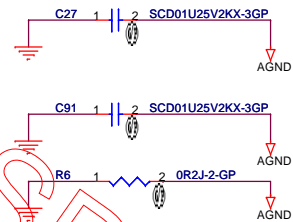
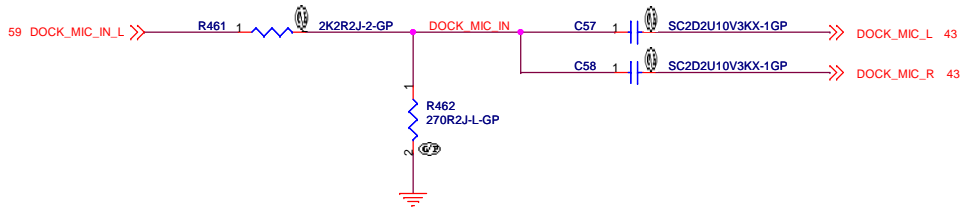
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緯創資通 Wistron Corporation
21E, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

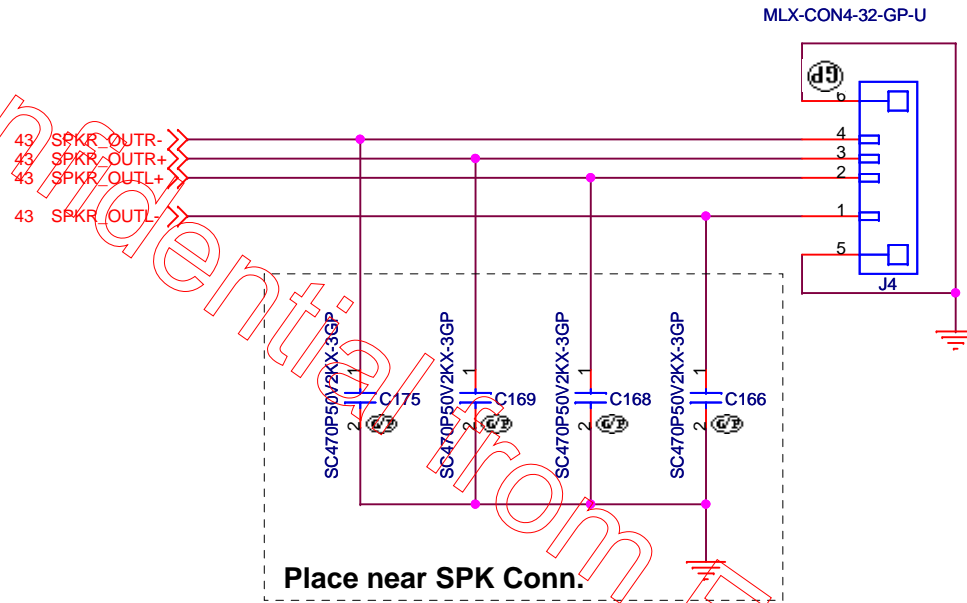
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Size	Document Number	Rev	
A3	SHINAI-4 UMA	-1	
Date:	Monday, March 12, 2012	Sheet	44 of 100



NEAR EXT MIC CONN



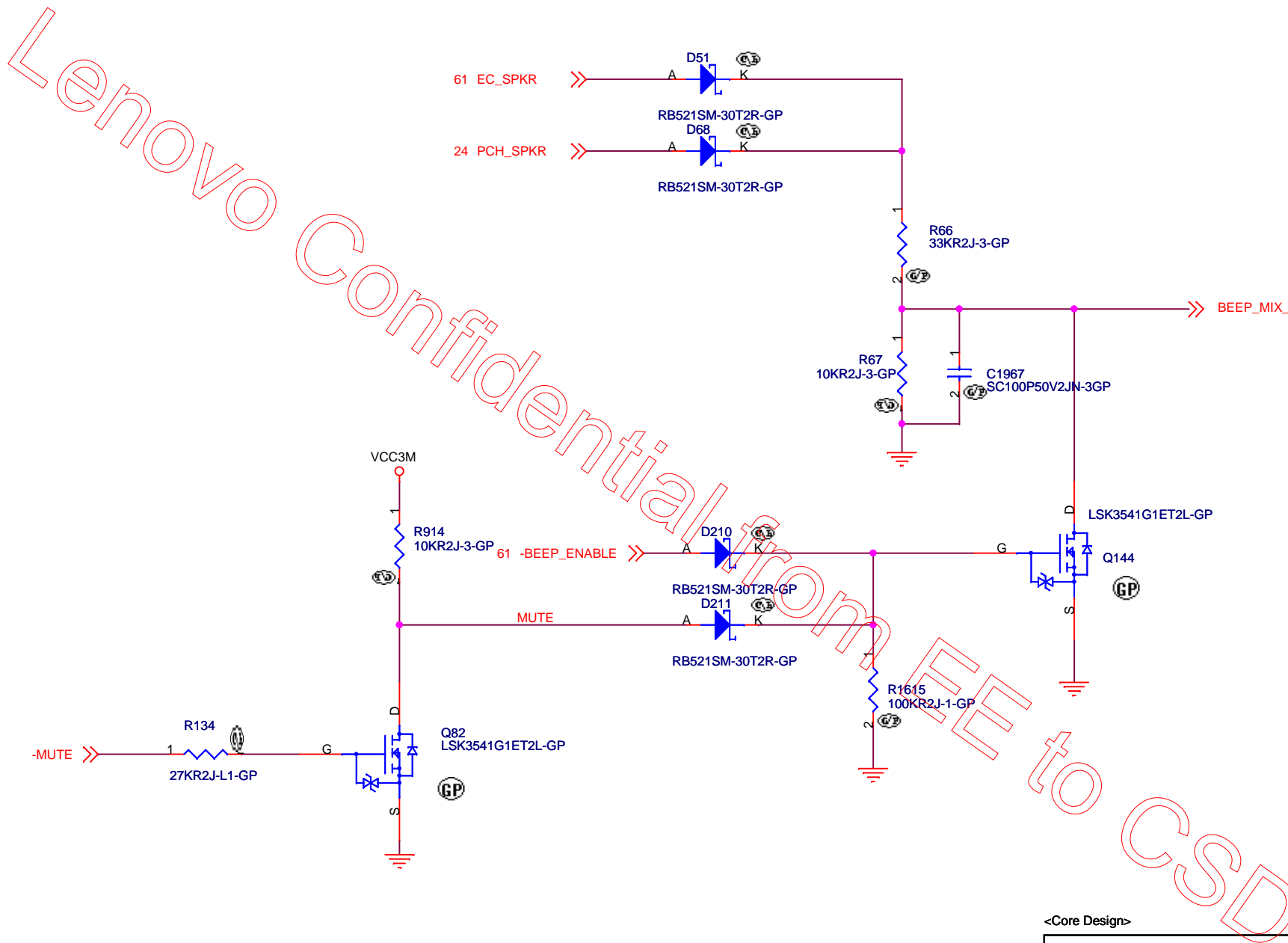
Lenovo Confidential from EFT to CSD



To utilize same speaker as SN3, SPKR_OUTL+ and SPKR_OUTL- are swapped.

<Core Design>

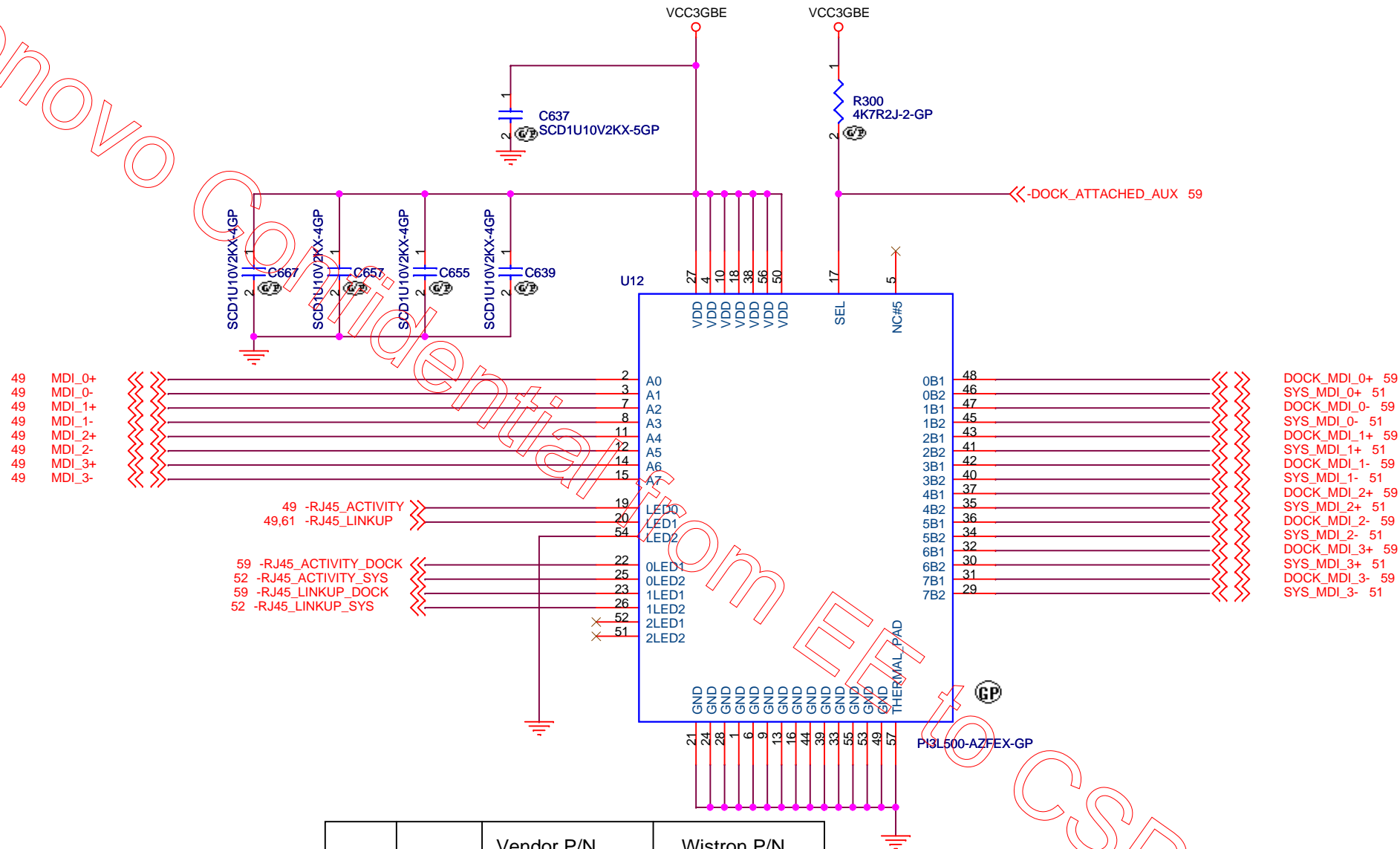
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title AUDIO SPEAKER		
Size A4	Document Number SHINAI-4 UMA	Rev -1
Date: Monday, March 12, 2012 Sheet 47 of 100		



<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Audio BEEP			
Size A4	Document Number		Rev -1
SHINAI-4 UMA			
Date: Monday, March 12, 2012	Sheet	48 of	100

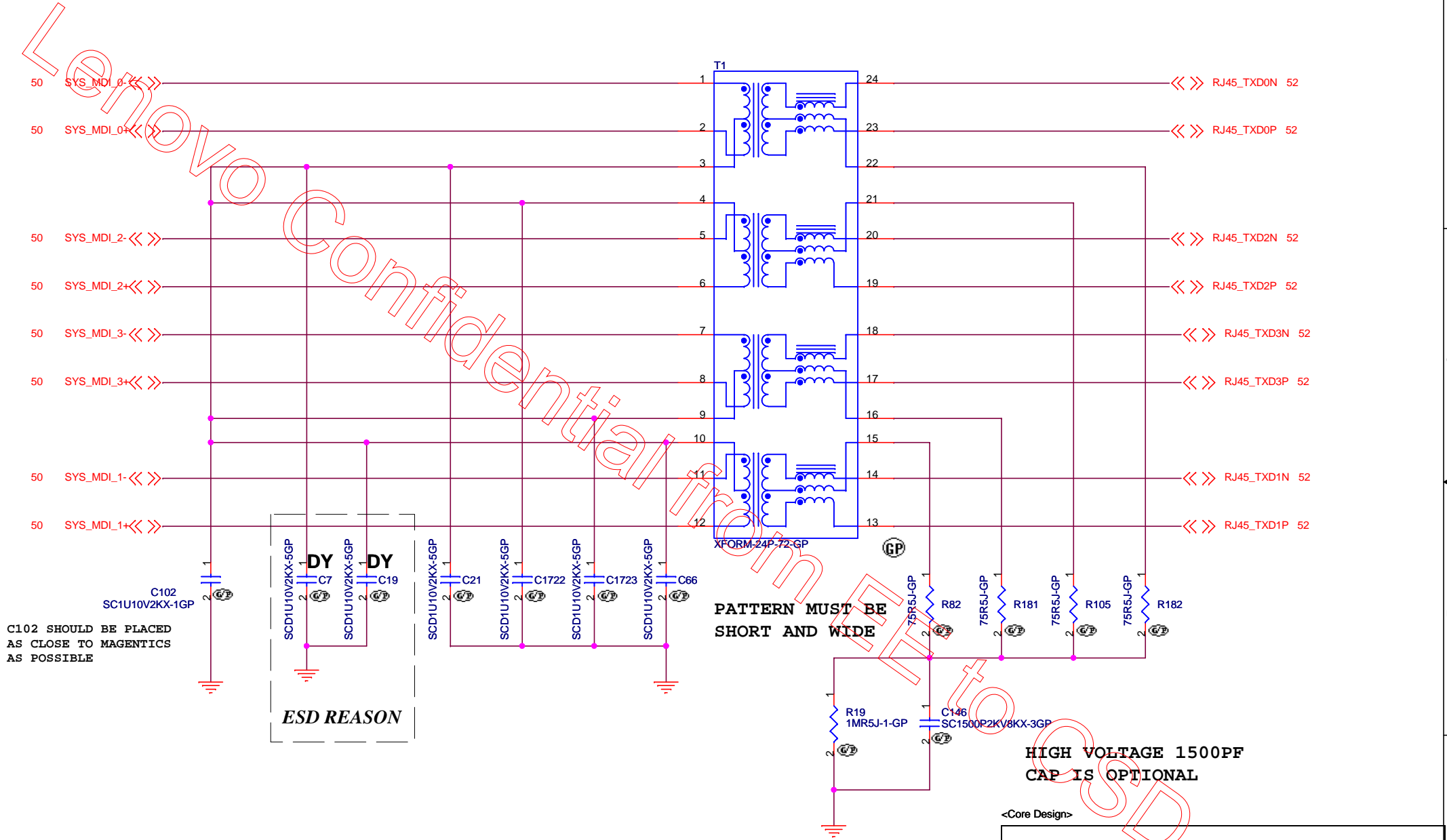
Lenovo



		Vendor P/N	Wistron P/N
1st	Pericom	PI3L500AZFEX	73.3L500.003
2nd	TI	TS3L500AERHUR	73.3L500.A0V
3rd	ST	STMUX1800LQTR	73.01800.003

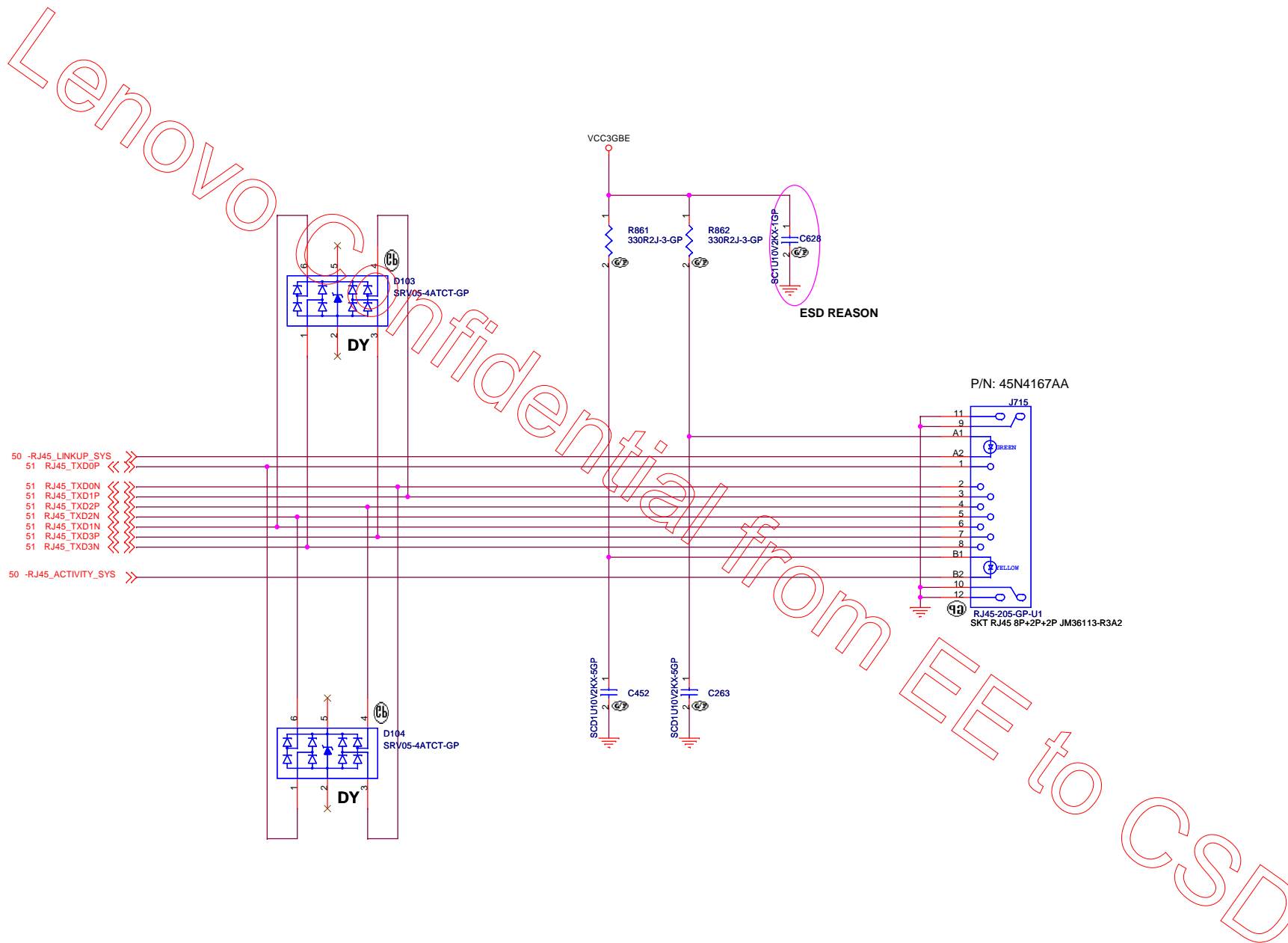
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緯創資通			Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.					
Title					
GBE LAN Switch					
Size	Document Number				Rev
A4	SHINAI-4 UMA				-1
Date: Monday, March 12, 2012		Sheet 50 of 100			



<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
GBE MAGNETICS			
Size	Document Number	Rev	
Custom		-1	
SHINAI-4 UMA			
Date:	Monday, March 12, 2012	Sheet	51 of 100



<Core Design>

緯創資通

Wistron Corporation
24F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RJ45 CONNECTOR

Size
A3

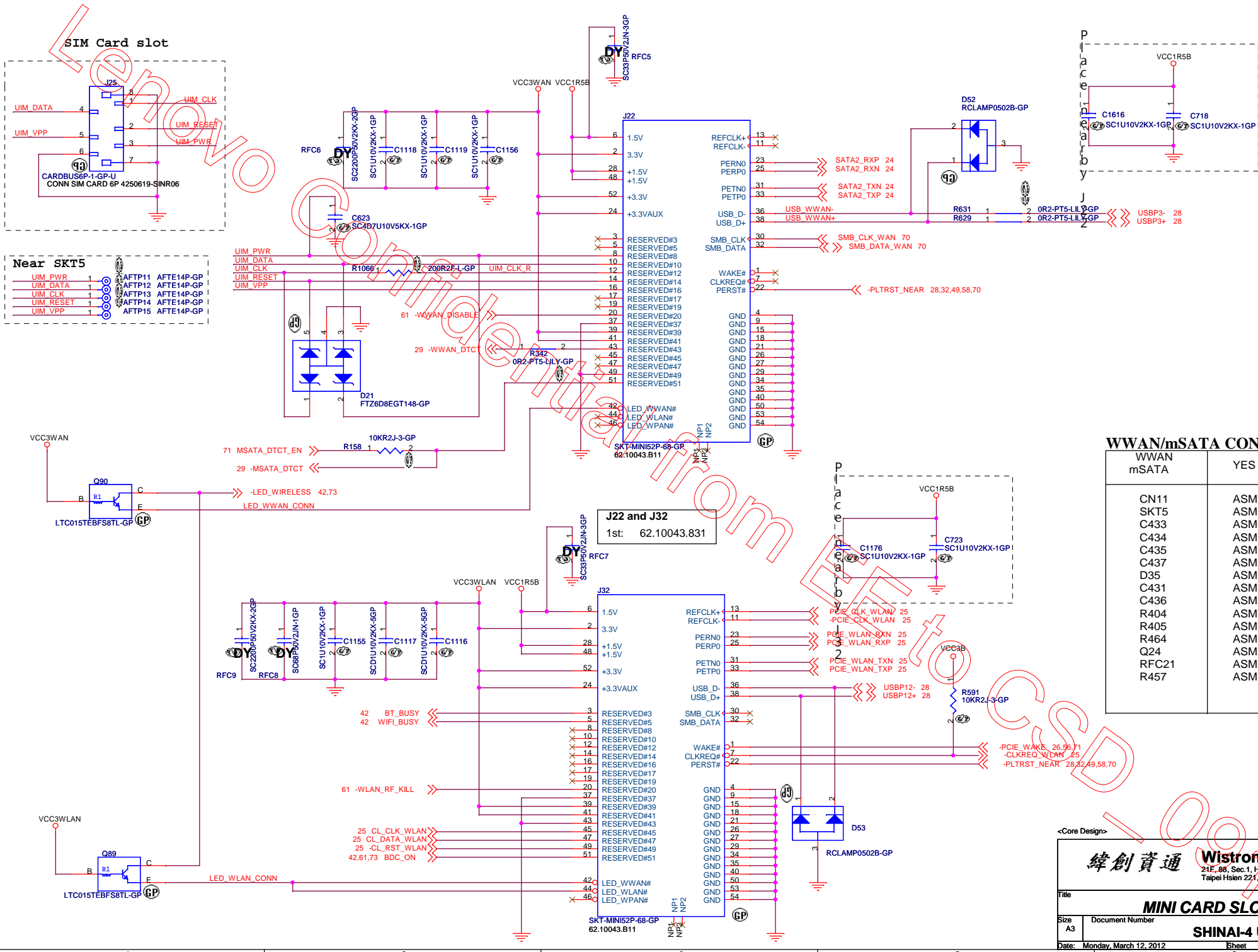
Document Number

SHINAI-4 UMA

Rev
-1

Date: Monday, March 12, 2012

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WWAN/mSATA CONTROL TABLE

WWAN mSATA	YES	NO
CN11	ASM	DY
SKT5	ASM	DY
C433	ASM	DY
C434	ASM	DY
C435	ASM	DY
C437	ASM	DY
D35	ASM	DY
C431	ASM	DY
C436	ASM	DY
R404	ASM	DY
R405	ASM	DY
R464	ASM	DY
Q24	ASM	DY
RFC21	ASM	DY
R457	ASM	DY

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BLANK

<Core Design>

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
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Size	Document Number		Rev
A4	SHINAI-4 UMA		-1
Date: Tuesday, March 06, 2012		Sheet 54 of	100

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<Core Design>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
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Size	Document Number	Rev
A4	SHINAI-4 UMA	-1
Date: Tuesday, March 06, 2012		Sheet 55 of 100

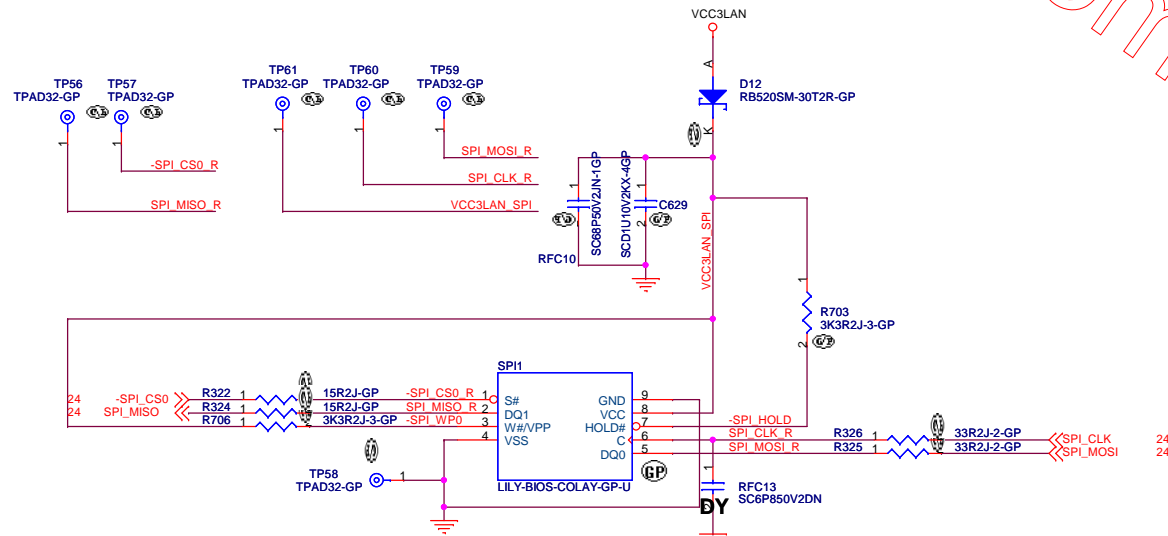
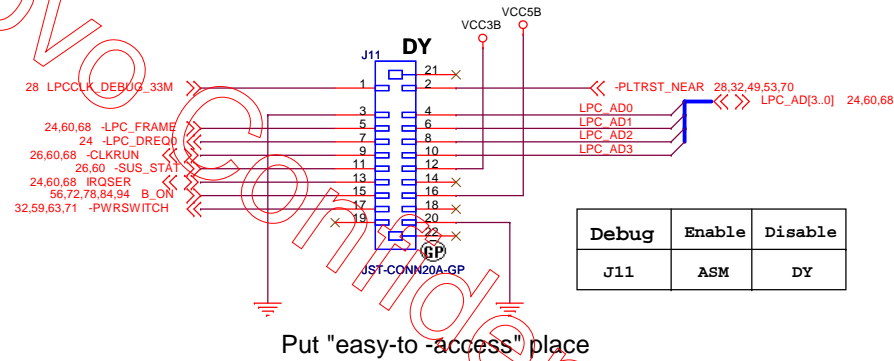
Lenovo Confidential from EE to CSD 0979

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<Core Design>

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Title BLANK			
Size A	Document Number SHINAI-4 UMA		Rev -1
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Debug card connector



Dual foot print for WSON and SO8

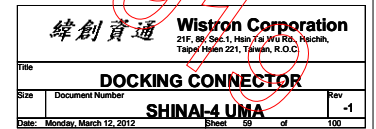
16MB			
WSON	Marconix	MX25L12835EZNI-10G	72.25128.X01
	Winbond	W25Q128BVEIG	72.25128.I01
	EON	EN25QH128-104YIP	72.25128.C03

SF100 PIN HEADER INTERFACE (TOP VIEW)			
1 VCC	D12.1	2 GND	GND
3 CS#	R322.2	3 CLK	R326.1
5 MISO	R324.2	5 MOSI	R325.1
7 (KEY)	N/A	7 (RESET)	N/A

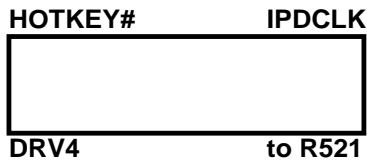
<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	SPI&LPC debug card
Size A3	Document Number
Date: Monday, March 12, 2012	Sheet 58 of 100
SHINAI-4 UMA Rev -1	

LOCAL	WISTRON	NET
149	1A	DOCK_PWR20_IN
150	2A	DOCK_PWR20_IN
151	3A	GND
152	4A	GND
153	5A	S_BAT_IN
154	6A	S_BAT_IN
155	7A	NA
156	8A	NA
157	149	GND
158	150	GND
159	151	GND
160	152	GND
161	153	GND
162	154	GND
163	NP1	NA
164	NP2	NA



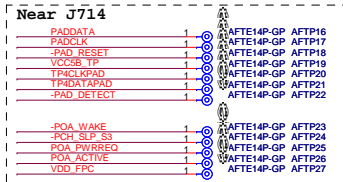
5

[illegible]

near by J7

緯創資通

Title			
KEYBOARD CONNECTOR			
Size	Document Number	Rev	
Custom	SHINAI-4 UMA	-1	
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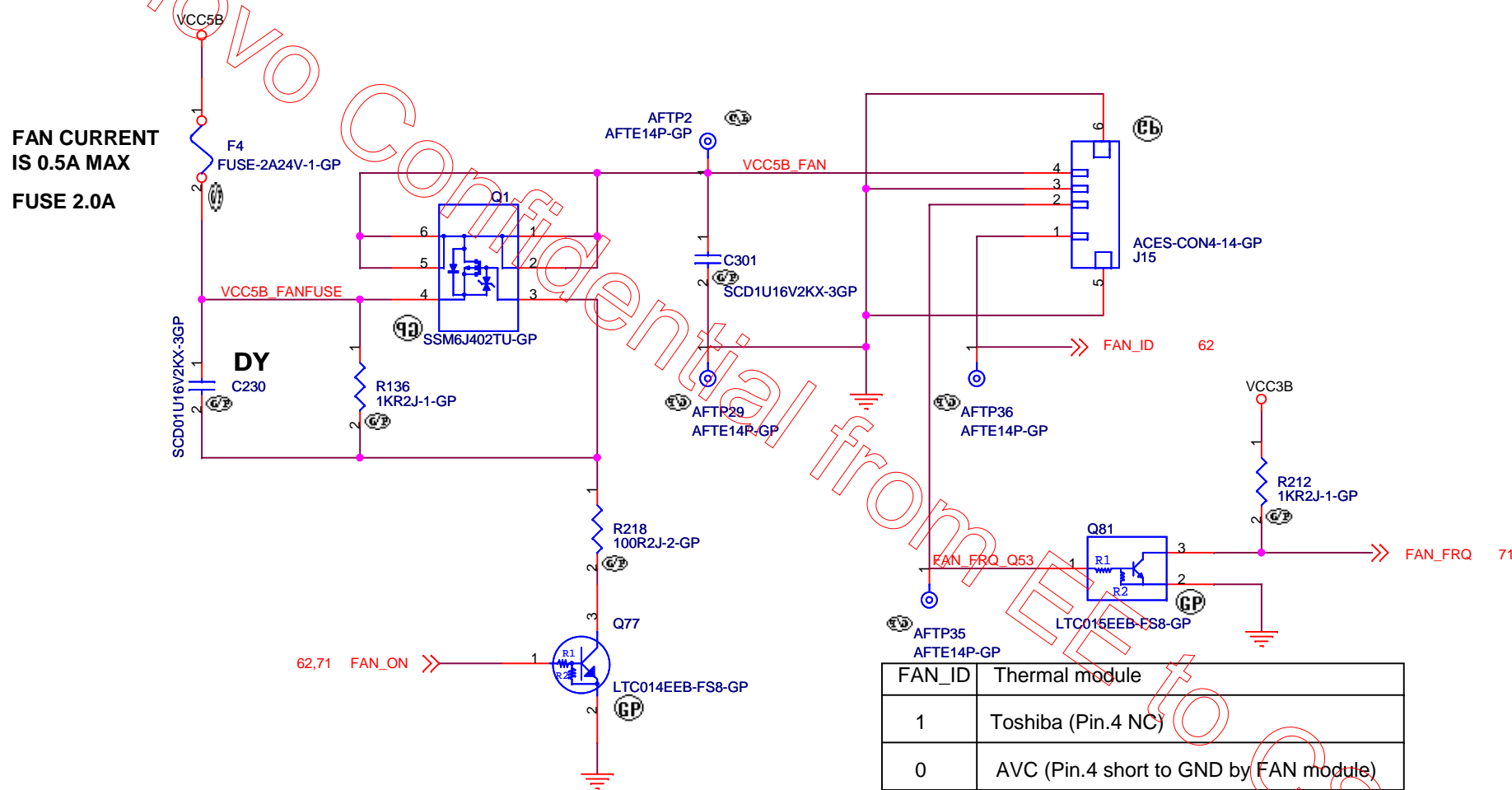
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<Core Design>

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Title BLANK			
Size A	Document Number SHINAI-4 UMA		Rev -1
Date: Tuesday, March 06, 2012		Sheet 65 of	100



<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

FAN Control

Size
A4

Document Number

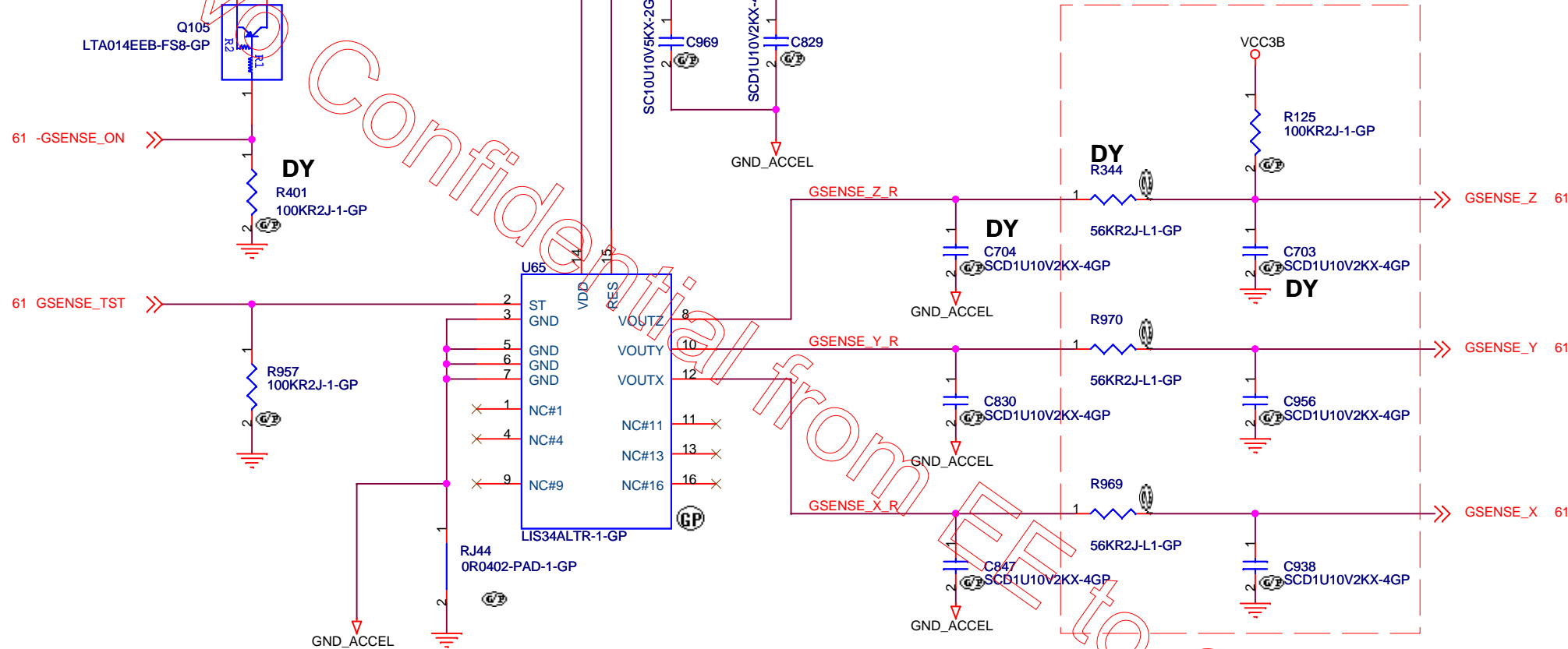
SHINAI-4 UMA

Rev	-1
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Date: Monday, March 12, 2012

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Lenovo



U38

Primary	STMicro LIS34AL	41R0828AA
Second	Kionix KXTC8-2850	74.KXTC8.0BZ
Third		

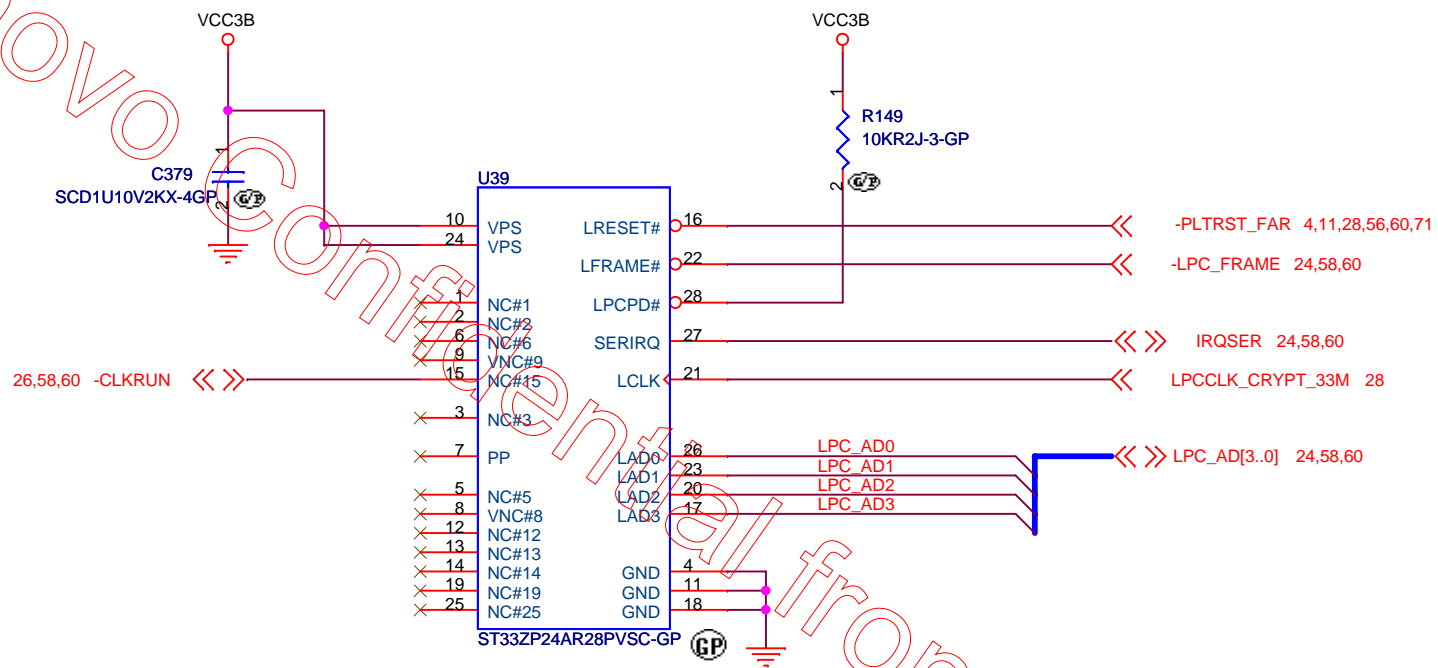
Layout Comment :

(1) Avoid routing under DCDC switching area.

Width = 6 mil & Spacing = 10 mil
for three Output traces

<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
G-SENSOR		
Size A4	Document Number	Rev -1
SHINAI-4 UMA		
Date: Monday, March 12, 2012	Sheet 67	of 100



SDV, FVT	ST33ZP24AR28PVRC-GP
FROM SIT	ST33ZP24AR28PVSC-GP

<Core Design>

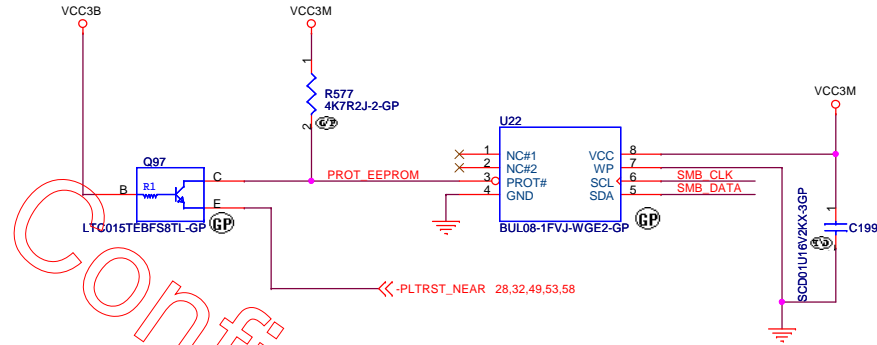
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Title		TPM	
Size A4	Document Number	SHINAI-4 UMA	
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<Variant Name>		
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Size A4	Document Number SHINAI-4 UMA	Rev -1
Date: Tuesday, March 06, 2012		Sheet 69 of 100

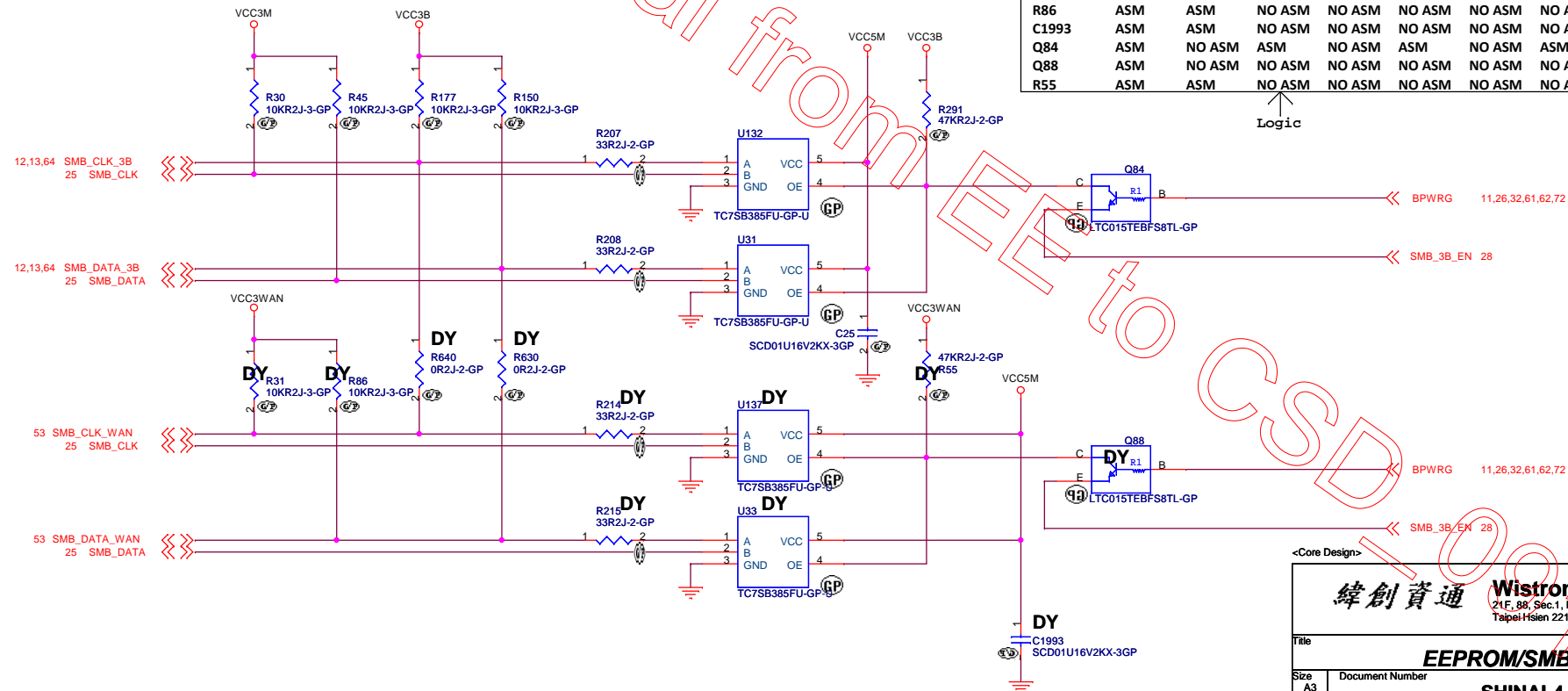
EEPROM



	Vendor	U22	Part Number
1st	ROHM	BUL08-1FVJ-W	72.BUL08.A0Q
2nd	NXP	PCA24S08ADP	72.24S08.A0Q
3rd	Sanyo	LE26CAP08TT	72.26C08.00R

AOAC	YES	YES	YES	YES	NO	NO	NO	NO
Anti Theft	YES	YES	NO	NO	YES	YES	NO	NO
EEPROM	U22	U23	U22	U23	U22	U23	U22	U23
U137	ASM	ASM	NO ASM	NO ASM	NO ASM	NO ASM	NO ASM	NO ASM
U33	ASM	ASM	NO ASM	NO ASM	NO ASM	NO ASM	NO ASM	NO ASM
R214	ASM	ASM	NO ASM	NO ASM	NO ASM	NO ASM	NO ASM	NO ASM
R215	ASM	ASM	NO ASM	NO ASM	NO ASM	NO ASM	NO ASM	NO ASM
R640	NO ASM	NO ASM	NO ASM	NO ASM	ASM	ASM	NO ASM	NO ASM
R630	NO ASM	NO ASM	NO ASM	NO ASM	ASM	ASM	NO ASM	NO ASM
R31	ASM	ASM	NO ASM	NO ASM	NO ASM	NO ASM	NO ASM	NO ASM
R86	ASM	ASM	NO ASM	NO ASM	NO ASM	NO ASM	NO ASM	NO ASM
C1993	ASM	ASM	NO ASM	NO ASM	NO ASM	NO ASM	NO ASM	NO ASM
Q84	ASM	NO ASM	ASM	NO ASM	NO ASM	NO ASM	ASM	NO ASM
Q88	ASM	NO ASM	NO ASM	NO ASM	NO ASM	NO ASM	NO ASM	NO ASM
R55	ASM	ASM	NO ASM	NO ASM	NO ASM	NO ASM	NO ASM	NO ASM

Logic



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **EEPROM/SMBUS SW**

Size: A3 Document Number: **SHINAI-4 UMA** Rev: -1

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AC_Present Pin has Open Drain type output buffer.

MISC_RST# is NC on KN4

MON is NC on KN4.

S_TRCL is added as SN3 design.
DB2 did not have this signal.

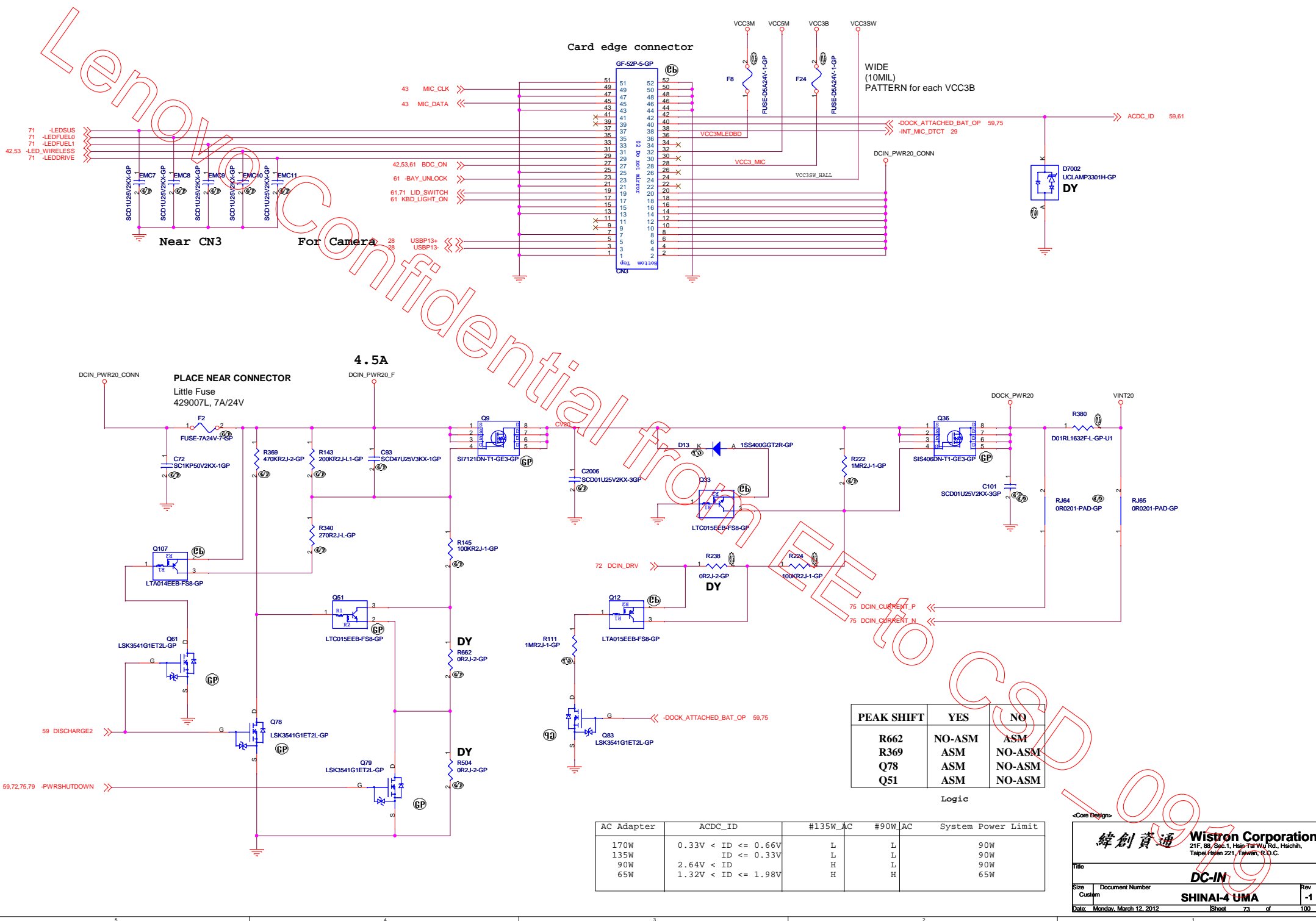
SW_RST is used to reset internal LDO.

<Variant Name>

緯創資通 Wistron Corporation
21F, 8F, Sec.1, Hsin Tai Wu Rd., Hsinchu,
Taipai Hsien 221, Taiwan, R.O.C.

Title Think Engine 1/2

Size	Document Number	Rev
Custm	SHINAI-4 UMA	-1
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PEAK SHIFT	YES	NO
R662	NO-ASM	ASM
R369	ASM	NO-ASM
Q78	ASM	NO-ASM
Q51	ASM	NO-ASM

Logic

AC Adapter	ACDC_ID	#135W_AC	#90W_AC	System Power Limit
170W	0.33V < ID <= 0.66V	L	L	90W
135W	ID <= 0.33V	L	L	90W
90W	2.64V < ID	H	L	90W
65W	1.32V < ID <= 1.98V	H	H	65W

緯創資通

Wistron Corporation

21F, 88, Sec. 1, Hsin-Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.

Title

DC-IN

Size

Document Number

SHINAI-4 UMA

Rev

-1

Date

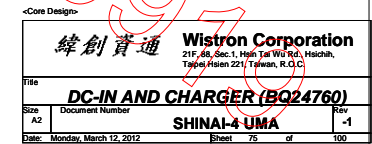
Monday, March 12, 2012

Sheet

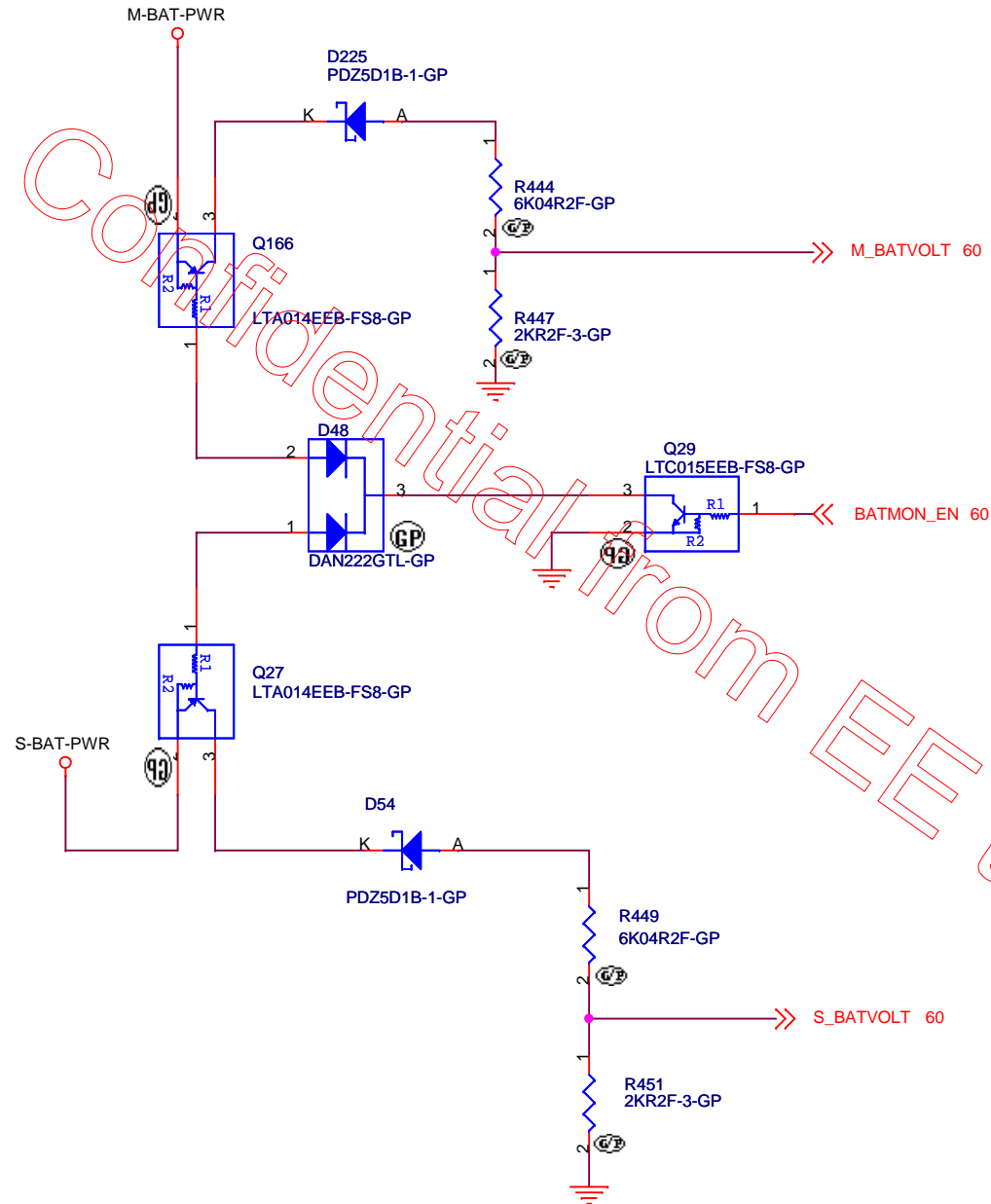
73

of

100



$V_{OUT} = 0.249 (V_{BAT} - 5)$



<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

BATTERY MONITOR

Size
A4

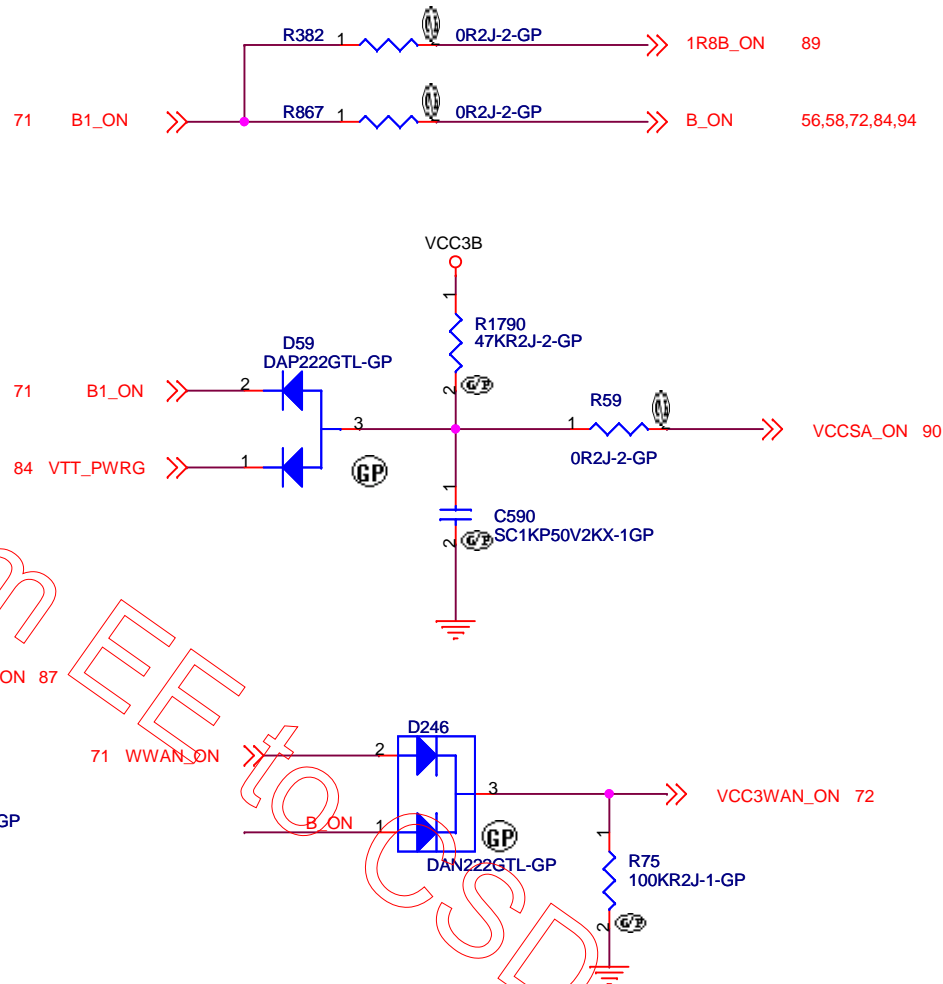
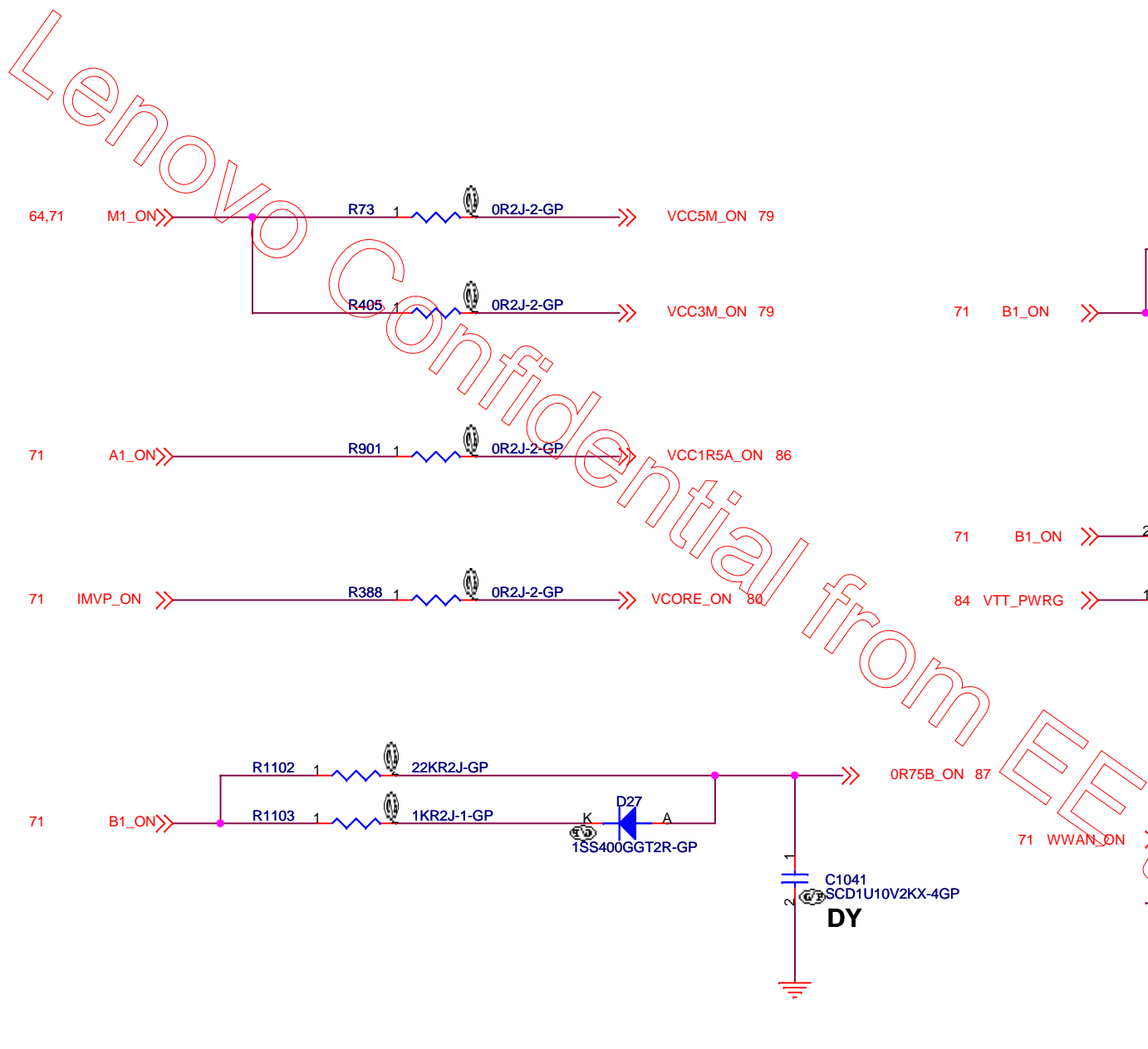
Document Number

SHINAI-4 UMA

Rev
-1

Date: Monday, March 12, 2012

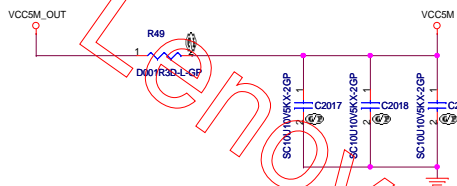
Sheet 77 of 100



<Core Design>

緯創資通			Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
POWER SEQUENCE					
Title		Document Number		Rev	
A4		SHINAI-4 UMA		-1	
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Layout R49 inside of L68



Input cap : 10uF 10% 25V X5R 8pcs.
These MLCCs must be placed
symmetrically on Top and Bottom.
Low Noise Cap

Input cap : 10uF 10% 25V X5R 4pcs.
These MLCCs must be placed
symmetrically on Top and Bottom.

Need common pad with
Toshiba, Infineon, Vishay, etc

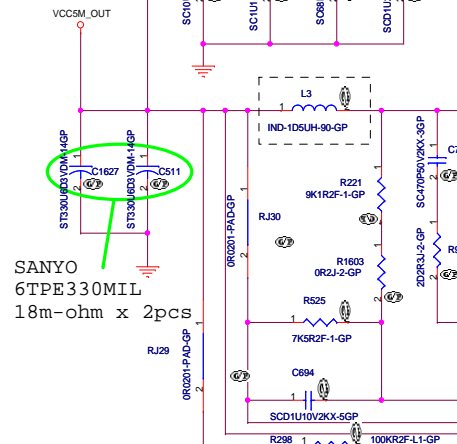
Q18
TPCC8064-H-GP
84.08064.037

Q17
TPCC8062-H-GP
84.08062.A37

L4

MPLCH0740L2R2 (NEC TOKIN)	68.2R21C.10T
SPM6540T-2R2M (TDK)	68.2R21E.10E

18A



SANYO
6TPE330MIL
18m-ohm x 2pcs

Need common pad with
Toshiba, Infineon, Vishay, etc

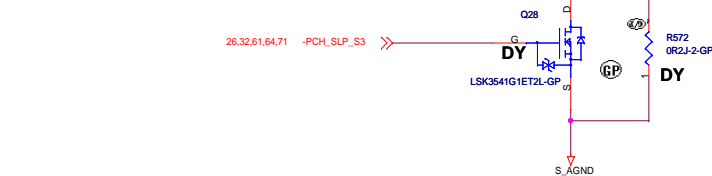
Q31, Q16
TPCC8064-H-GP
84.08064.037

Q50, Q46
TPCC8062-H-GP
84.08062.A37

L3

MPCH1055L1R3(NEC/TOKIN)	68.1R310.20A
FDU1050D-H-1R5M(TOKO)	68.1R51B.10K

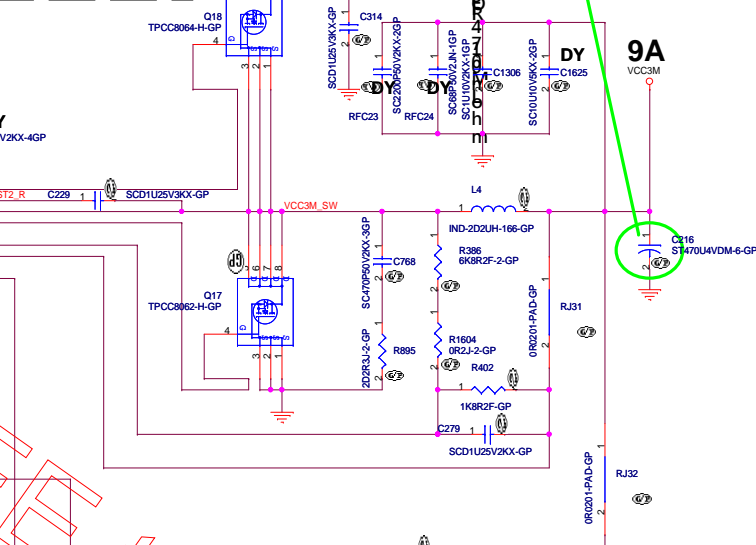
A



10UF 10% 25V X5R
8pcs

10UF 10% 25V X5R
4pcs

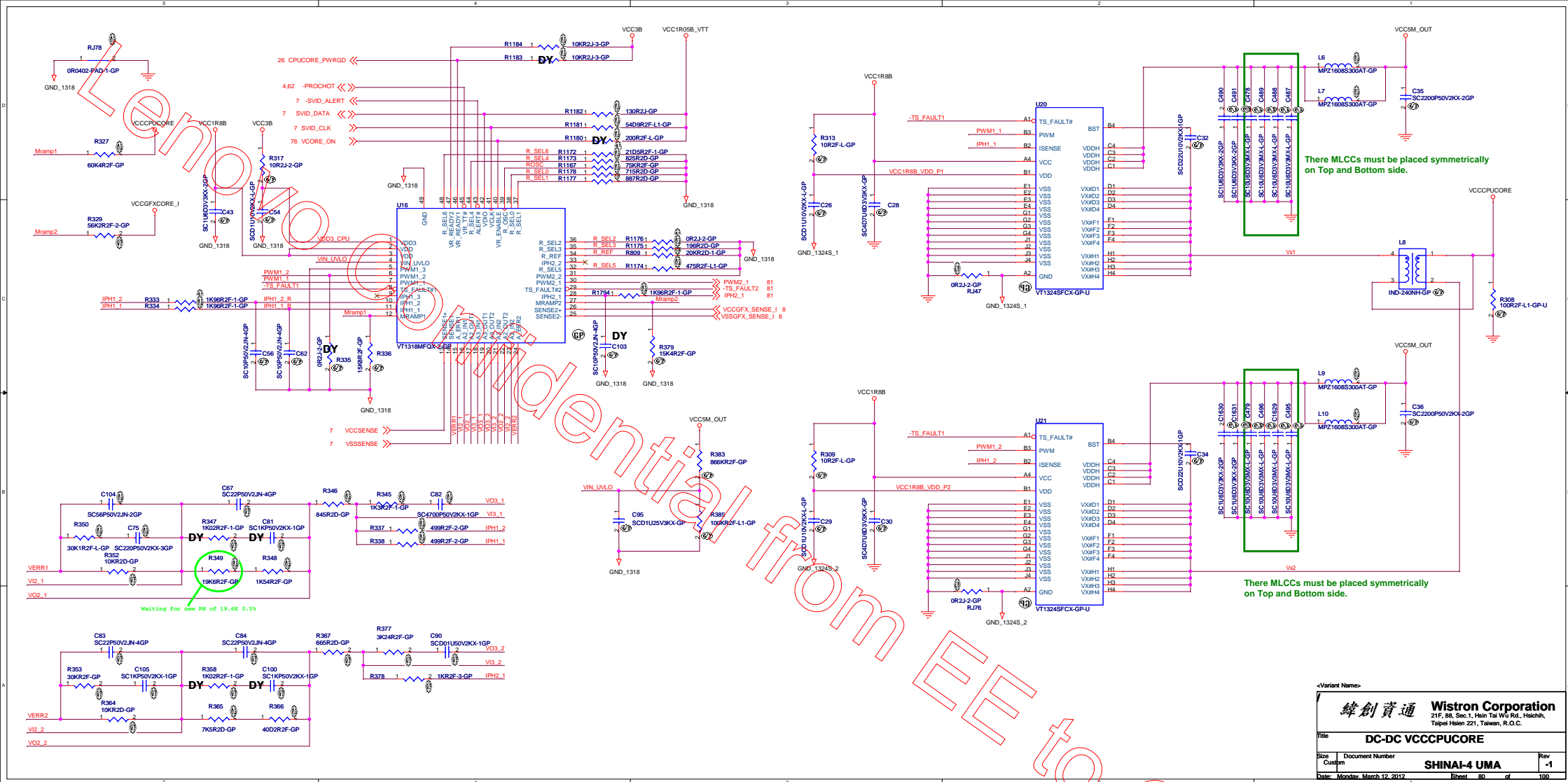
9A



<Core Design>

緯創資通 Wistron Corporation
23F, 88, Sec.1, Hsin Tsai Wu Rd., Hsinchu,
Taipei Hsein 221, Taiwan, R.O.C.

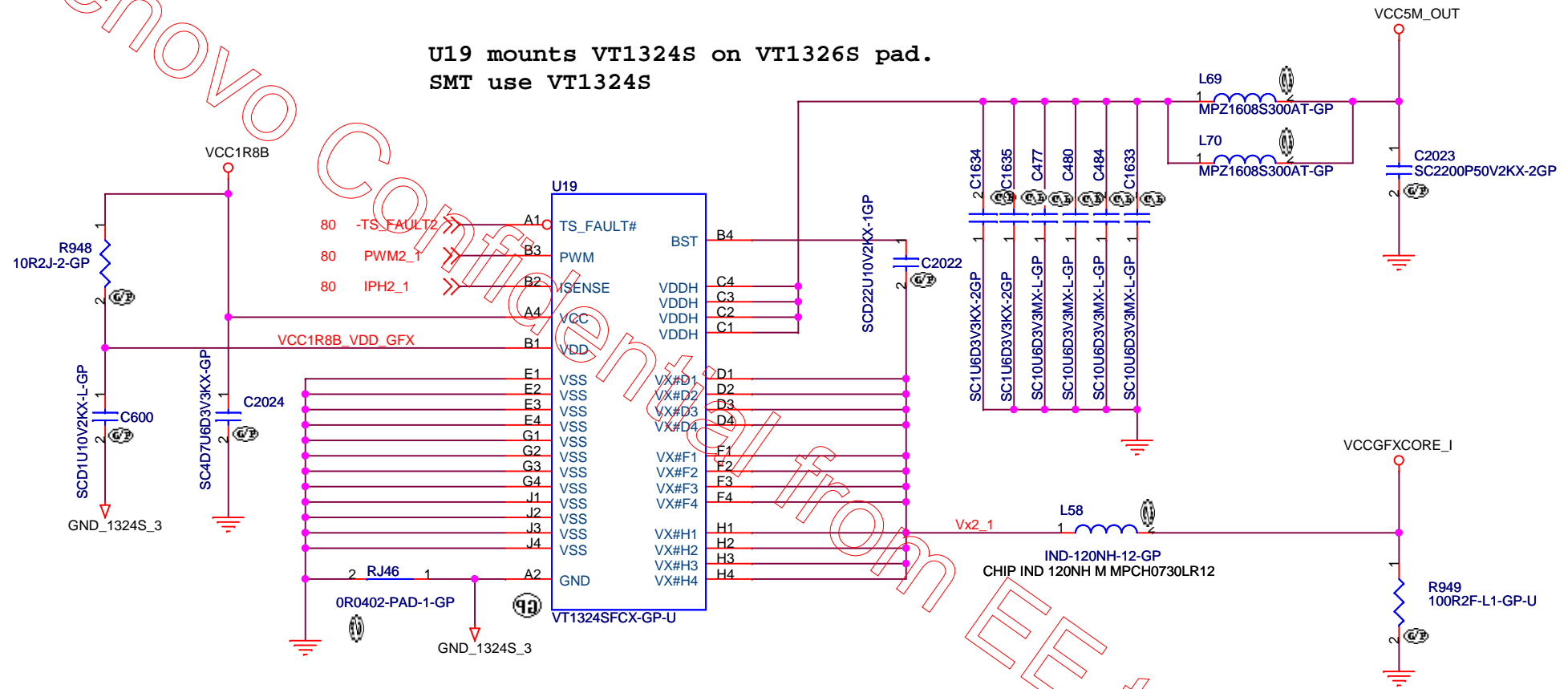
Title		DC-DC VCC3M/VCC5M	
Size	Document Number	Rev	-1
Customer	SHINAI-4 UMA		
Date	Monday, March 12, 2012	Sheet	79 of 100




Lenovo

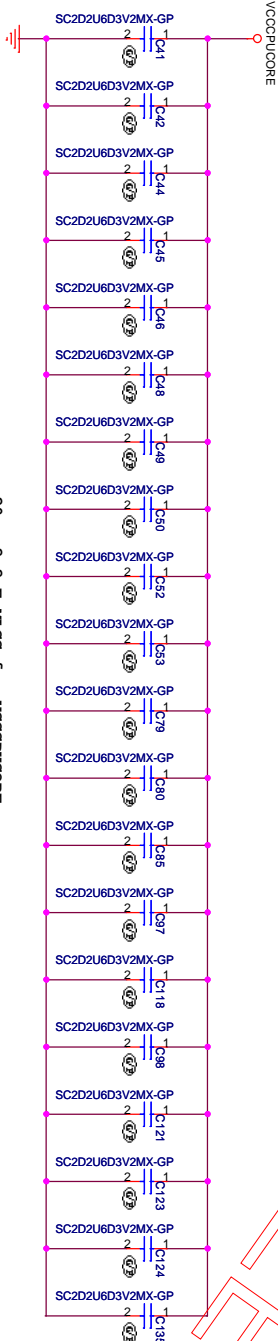
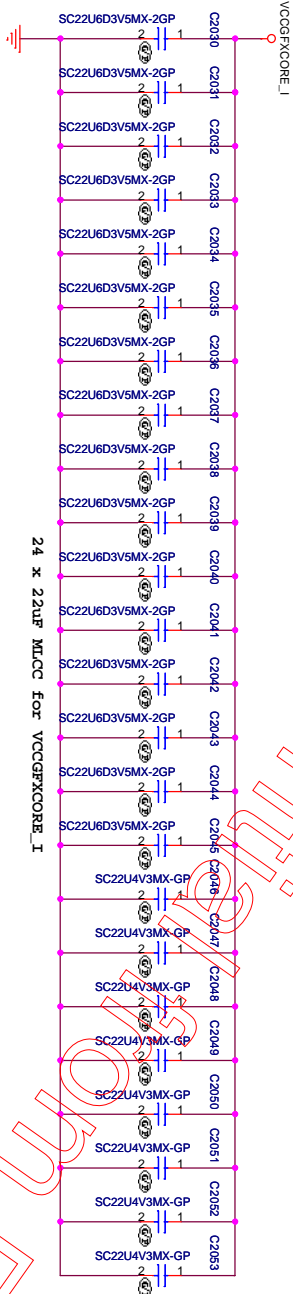
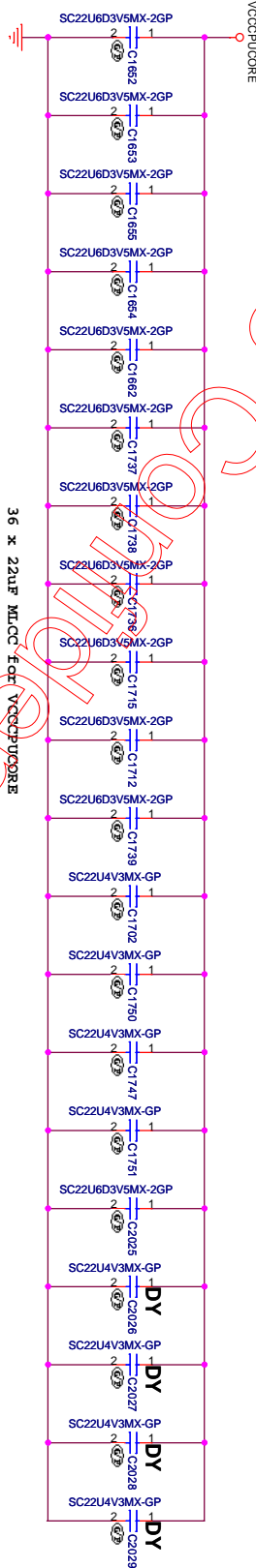
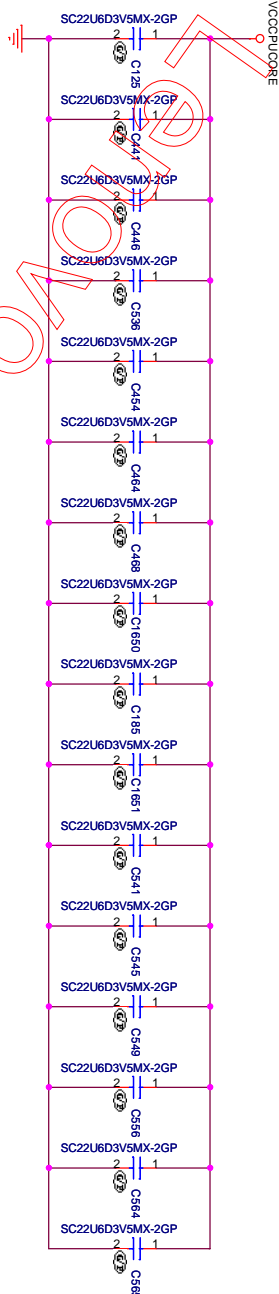
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U19 mounts VT1324S on VT1326S pad.
SMT use VT1324S



<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
VCCGFXCORE			
Size	Document Number		Rev
A4	SHINAI-4 UMA		-1
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<Core Design>

緯創資通

Wistron Corporation
2/F, 85, Sec.1, Hsin-Tai Wu Rd., Hsichih,
Tapei Hsien 227, Taiwan, R.O.C.

DC-DC VCCPUCORE

SHINAI-4 UMA

Date: Tuesday, March 06, 2012 Sheet: 82 of 100

VT1318M Parameters For Ivy Bridge

Master IC		SV	ULV
U48		VT1318M	VT1318M
# of slave for CPU	U47	2	2
Slave for CPU	U49	VT1324S	VT1324S
Inductor for CPU	L28	VT1324S	VT1324S
	L14	BPW10040	BPW10040
		no stuff	no stuff
# of slave for GPU	U50	1	1
Slave for GPU	L29	VT1324S	VT1324S
Inductor for GPU		MPCH0730LR12	MPCH0730LR12

		SV		ULV	
R_SEL[0]	pin 38	R1574	191	1.0%	147
R_SEL[1]	pin 37	R1575	215	1.0%	215
R_SEL[2]	pin 36	R1576	0	5.0%	0
R_SEL[3]	pin 35	R1577	191	1.0%	191
R_SEL[4]	pin 44	R1571	191	1.0%	191
R_SEL[5]	pin 32	R1579	374	1.0%	374
R_SEL[6]	pin 48	R1567	37.4	1.0%	37.4
R_REF	pin 34	R1578	20K	0.5%	20K
ROSC	pin 39	R1572	75K	1.0%	75K

			SV		ULV	
LL_R1_CPU	pin 15 - pin 16	R1599	10K	0.5%	10K	0.5%
LL_R2_CPU	pin 16 - pin 17	R1600	17.4K	0.5%	16.5K	0.5%
	pin 16 - pin 17	R1601	0	5.0%	0	5.0%
LL_C1_CPU	pin 15 - pin 16	C1086	22pF		22pF	
LL_C2_CPU	pin 16 - pin 17	C1087	22pF		22pF	
LL_RLEAD_CPU	pin 15 - pin 16	R1595	13K	1.0%	13K	1.0%
LL_CLEAD_CPU	pin 15 - pin 16	C1091	1000pF		1000pF	
LL_RLAG_CPU	pin 16 - pin 17	R1596	no stuff		no stuff	
LL_CLAG_CPU	pin 16 - pin 17	C1092	no stuff		no stuff	
RDES_CPU	pin 17 - pin 18	R1592	665	0.5%	976	0.5%
RINT_CPU	pin 18 - pin 19	R1593	665	1.0%	665	1.0%
CINT_CPU	pin 18 - pin 19	C1088	10nF		10nF	
RPH11	IPH1_1 - pin 18	R1594	1.02K	1.0%	1.02K	1.0%
RPH12	IPH1_2 - pin 18	R1598	1.02K	1.0%	1.02K	1.0%
IPHF11_R	pin 11	R1582	1.96K	1.0%	1.96K	1.0%
IPHF11_C	pin 11	C1076	10pF		10pF	
IPHF12_R	pin 10	R1581	1.96K	1.0%	1.96K	1.0%
IPHF12_C	pin 10	C1075	10pF		10pF	
R_MRAMP1	pin 12	R1584	16.2K	1.0%	16K	
R_MRAMP1_PU	pin 12	R1587	no stuff		no stuff	1.0%
R_PWM2	Pin 6	R4	no stuff		no stuff	
LL_R1_GPU	pin 24 - pin 23	R1069	10K	0.5%	10K	0.5%
LL_R2_GPU	pin 23 - pin 22	R1610	8.25K	0.5%	8.25K	0.5%
	pin 23 - pin 22	R1611	0	5.0%	0	5.0%
LL_C1_GPU	pin 24 - pin 23	C1094	22pF		22pF	
LL_C2_GPU	pin 23 - pin 22	C1095	22pF		22pF	
LL_RLEAD_GPU	pin 24 - pin 23	R1606	30K	1.0%	30K	1.0%
LL_CLEAD_GPU	pin 24 - pin 23	C1097	1000pF		1000pF	
LL_RLAG_GPU	pin 23 - pin 22	R1607	no stuff		no stuff	
LL_CLAG_GPU	pin 23 - pin 22	C1098	no stuff		no stuff	
RDES_GPU	pin 22 - pin 21	R1604	665	0.5%	665	0.5%
RINT_GPU	pin 21 - pin 20	R1605	3.24K	1.0%	3.24K	1.0%
CINT_GPU	pin 21 - pin 20	C1096	10nF		10nF	
RPH21	IPH2_1 - pin 21	R1608	1K	1.0%	1K	1.0%
IPHF21_R	pin 28	R1580	1.96K	1.0%	1.96K	1.0%
IPHF21_C	pin 28	C1077	no stuff		no stuff	
R_MRAMP2	pin 27	R1586	15.4K	1.0%	15.4K	1.0%
R_MRAMP2_PU	pin 27	R1590	56.2K	1.0%	56.2K	1.0%

			SV	ULV
		C1090	4.7uF	4.7uF
		R1589	10 1.0%	10 1.0%
		C1089	0.1uF	0.1uF
		C1082	0.22uF	0.22uF
		C1083	1uF	1uF
		C1080	1uF	1uF
		C1084	10uF	10uF
		C1079	10uF	10uF
		C1081	10uF	10uF
		C1085	10uF	10uF
		L50	MPZ1608S300A	MPZ1608S300A
		L51	MPZ1608S300A	MPZ1608S300A
		C1087	2200pF	2200pF

Vcore Coutput

		SV		ULV	
C669	22uF	2125	22uF	2125	
C670	22uF	2125	22uF	2125	
C671	22uF	2125	22uF	2125	
C672	22uF	2125	22uF	2125	
C673	22uF	2125	22uF	2125	
C674	22uF	2125	22uF	2125	
C675	22uF	2125	22uF	2125	
C676	22uF	2125	22uF	2125	
C677	22uF	2125	22uF	2125	
C678	22uF	2125	22uF	2125	
C679	22uF	2125	22uF	2125	
C680	22uF	2125	22uF	2125	
C681	22uF	2125	22uF	2125	
C682	22uF	2125	22uF	2125	
C683	22uF	2125	22uF	2125	
C684	22uF	2125	22uF	2125	
C685	22uF	2125	22uF	2125	
C686	22uF	2125	22uF	2125	
C687	22uF	2125	22uF	2125	
C688	22uF	2125	22uF	2125	
C689	22uF	2125	22uF	2125	
C690	22uF	2125	22uF	2125	
C691	22uF	2125	N/A	2125	
C692	22uF	2125	N/A	2125	
C693	22uF	2125	N/A	2125	
C694	22uF	2125	N/A	2125	
C695	22uF	1608	N/A	1608	
C696	22uF	1608	N/A	1608	
C697	22uF	1608	N/A	1608	
C698	22uF	1608	N/A	1608	
C750	22uF	2125	N/A	2125	
C1109	22uF	2125	N/A	2125	
C1110	N/A	1608	N/A	1608	
C1111	N/A	1608	N/A	1608	
C1112	N/A	1608	N/A	1608	
C1113	N/A	1608	N/A	1608	

GFX Coutput

		SV		ULV	
C642	22uF	2125	22uF	2125	
C643	22uF	2125	22uF	2125	
C644	22uF	2125	22uF	2125	
C645	22uF	2125	22uF	2125	
C646	22uF	2125	22uF	2125	
C647	22uF	2125	22uF	2125	
C648	22uF	2125	22uF	2125	
C649	22uF	2125	22uF	2125	
C650	22uF	2125	22uF	2125	
C651	22uF	2125	22uF	2126	
C652	22uF	2125	22uF	2125	
C663	22uF	2125	22uF	2125	
C664	22uF	2125	22uF	2125	
C665	22uF	2125	22uF	2125	
C666	22uF	2125	22uF	2125	
C667	22uF	2125	22uF	2125	
C1114	22uF	1608	22uF	1608	
C1115	22uF	1608	22uF	1608	
C1116	22uF	1608	22uF	1608	
C1117	22uF	1608	22uF	1608	
C1118	22uF	1608	22uF	1608	
C1119	22uF	1608	22uF	1608	
C1120	22uF	1608	22uF	1608	
C1121	22uF	1608	22uF	1608	

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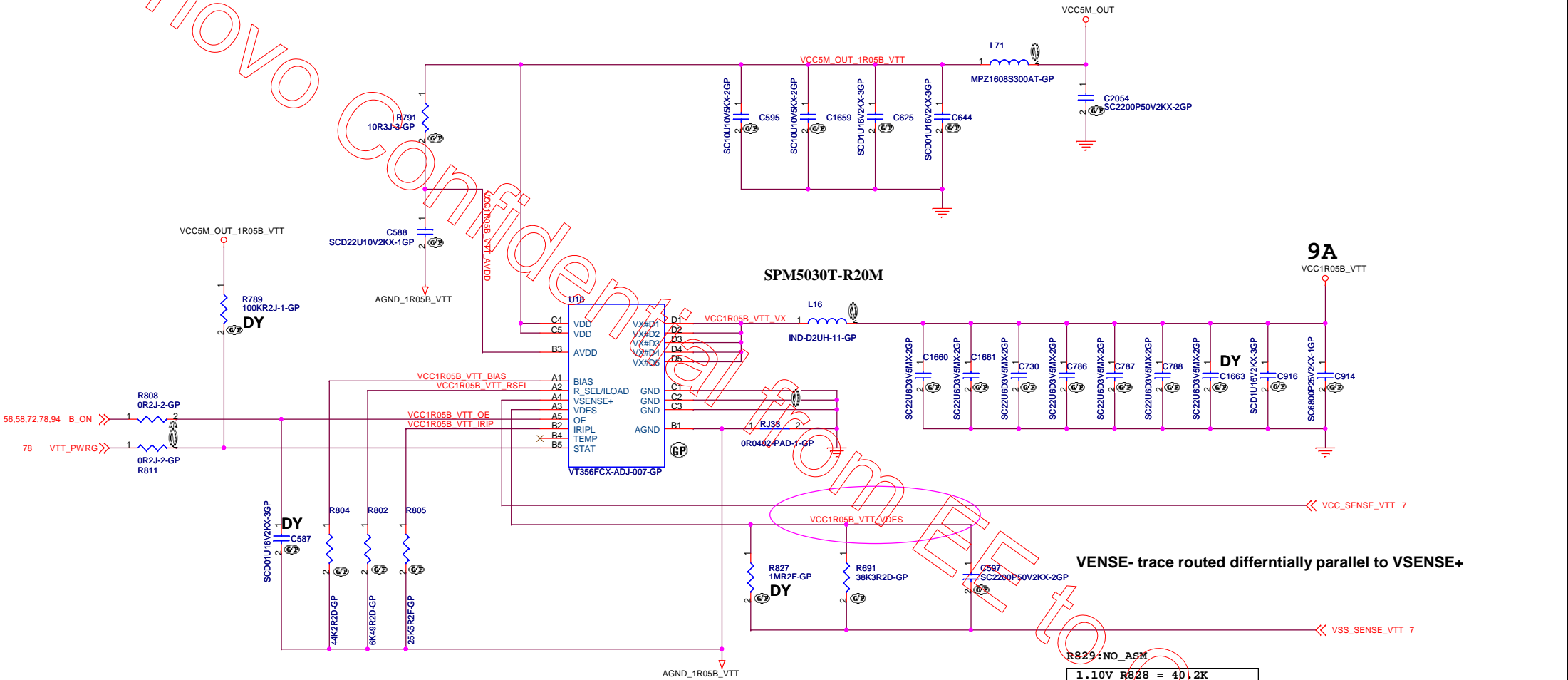
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.					
Title					
VT1318M TABLE					
Size	Document Number		Rev		
A3	SHINAI-4 UMA		-1		
Date: Tuesday, March 06, 2012		Sheet 83	of 100		

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SPM5030T-R20M

9A



VENSE- trace routed differentially parallel to VSENSE+

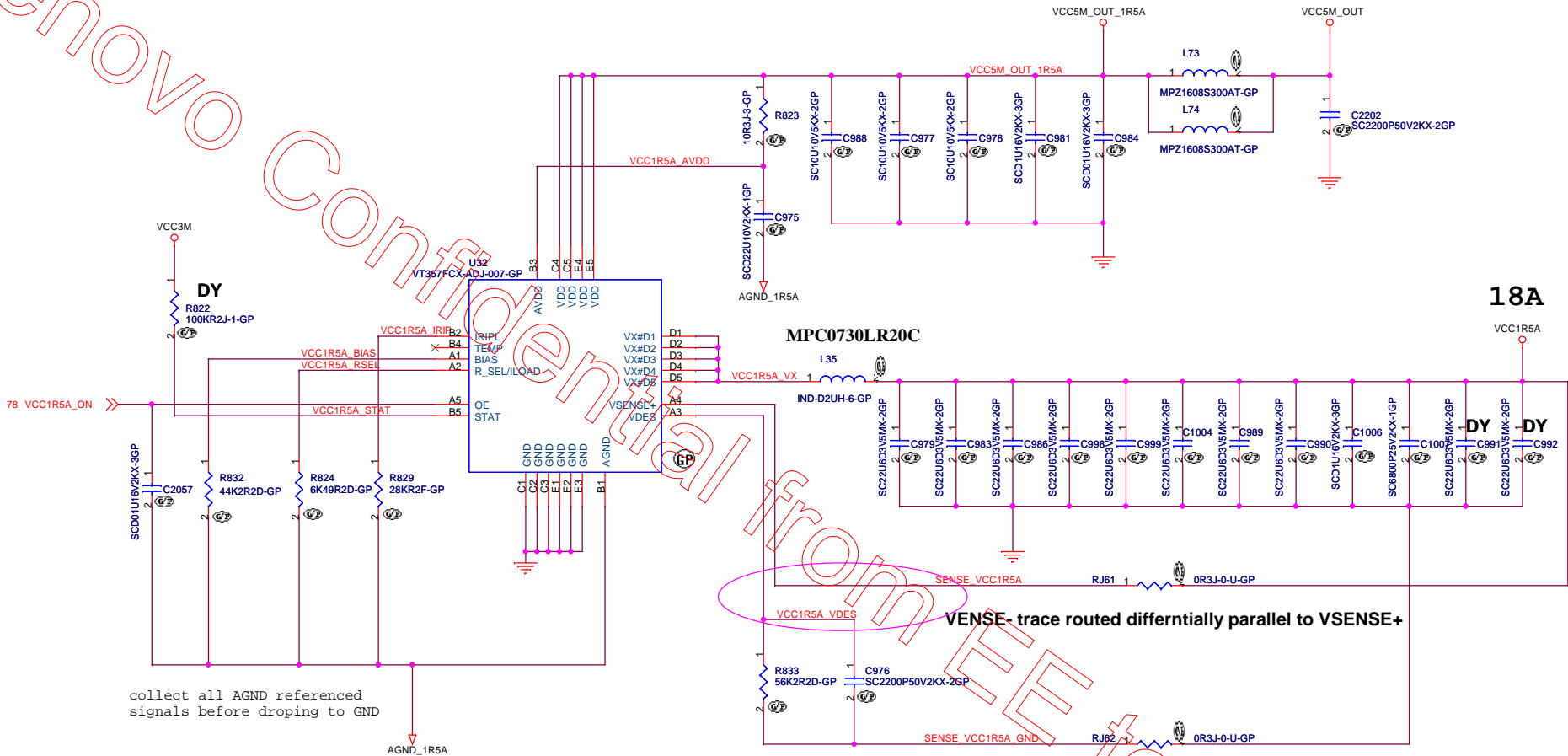
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 1.10V R828 = 40.2K
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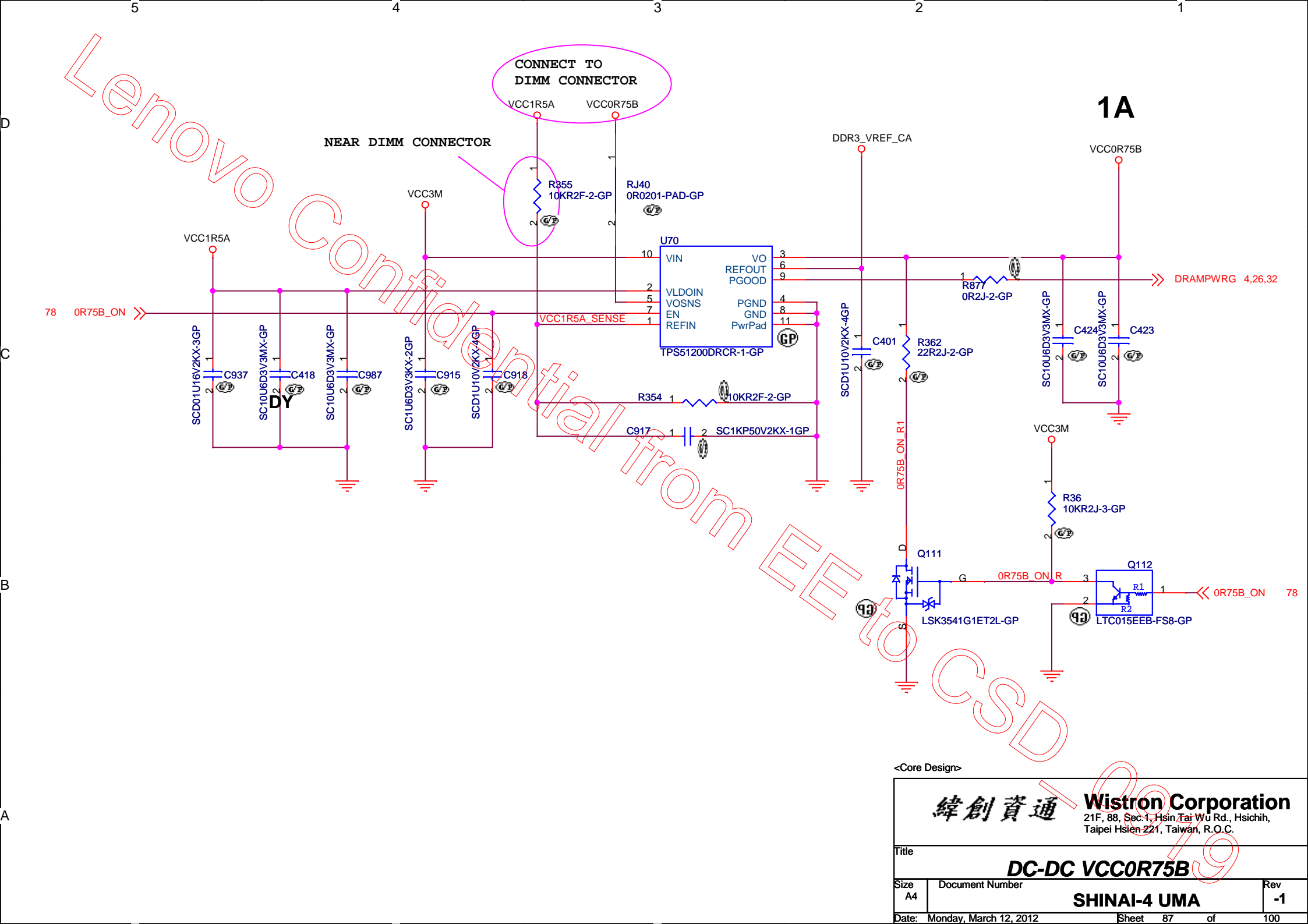
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from ESD to CSD





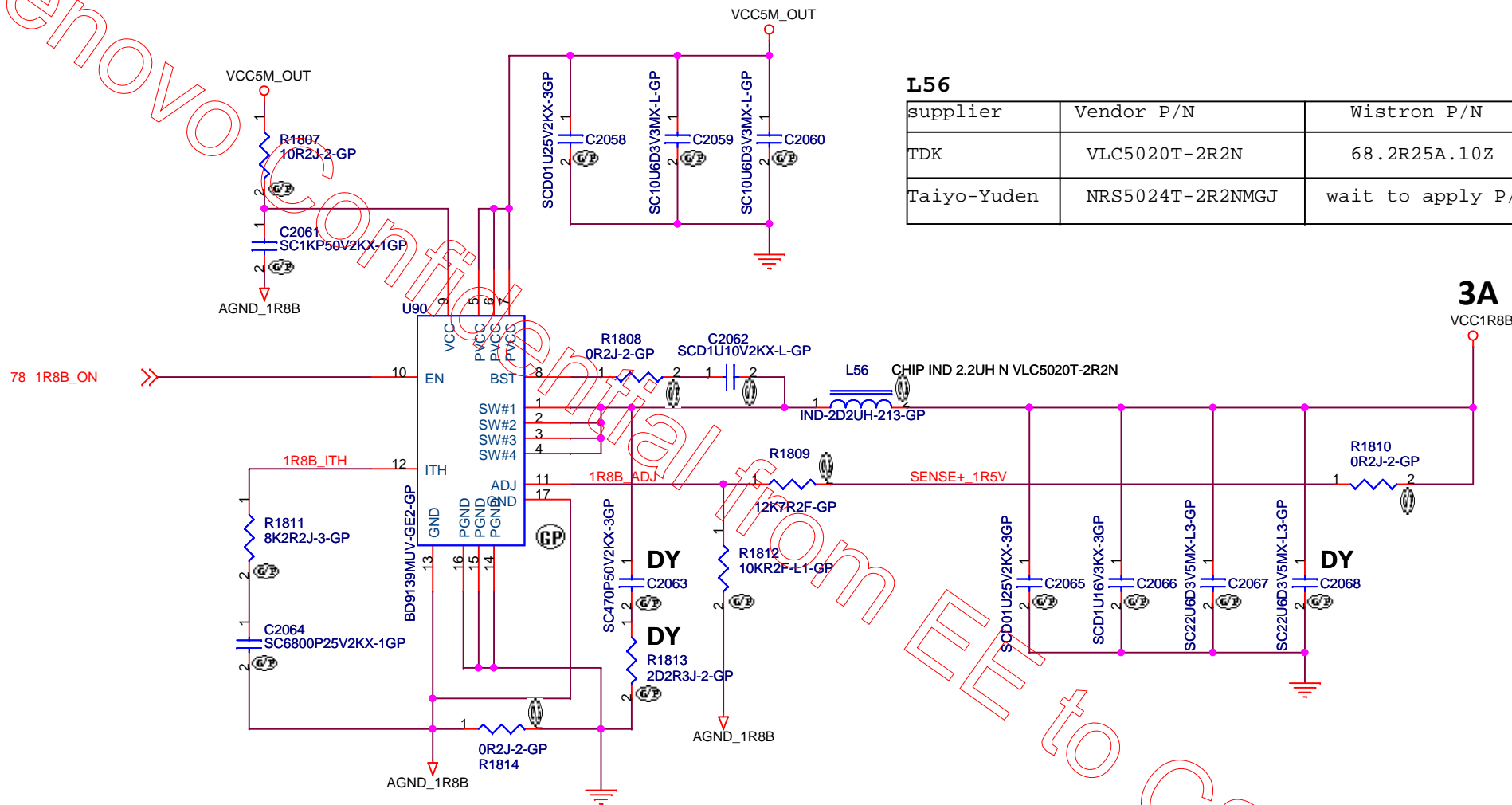
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Size A4	Document Number		Rev
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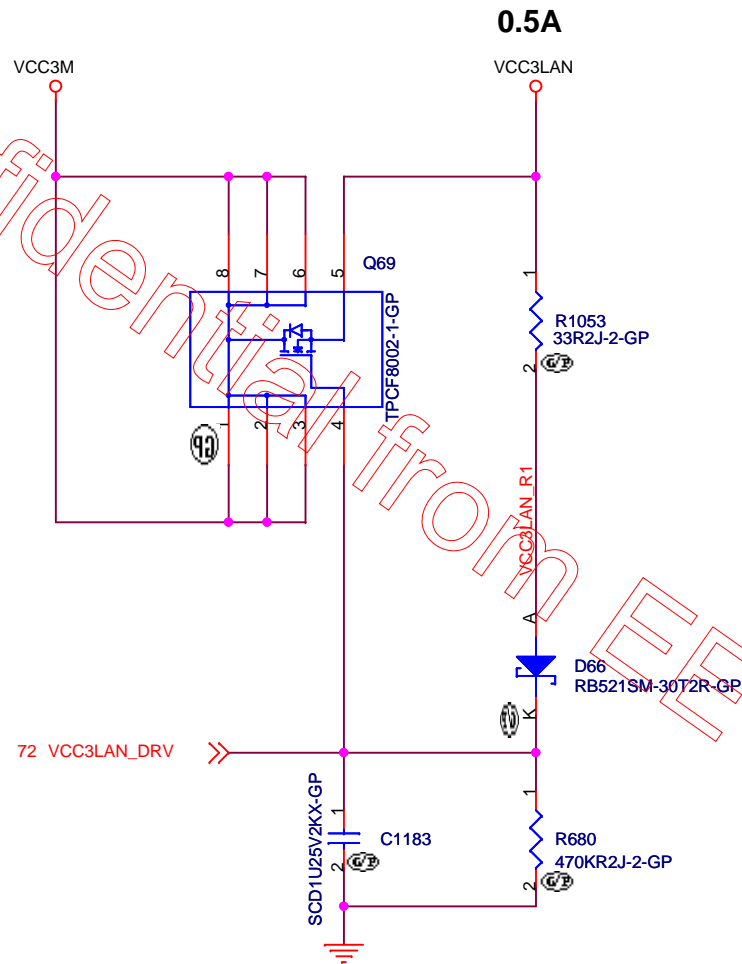
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supplier	Vendor P/N	Wistron P/N
TDK	VLC5020T-2R2N	68.2R25A.10Z
Taiyo-Yuden	NRS5024T-2R2NMGJ	wait to apply P/N

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<p>Date</p> <p>Monday, March 12, 2012</p>	<p>Sheet</p> <p>89 of 100</p>

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A4

Document Number

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-1

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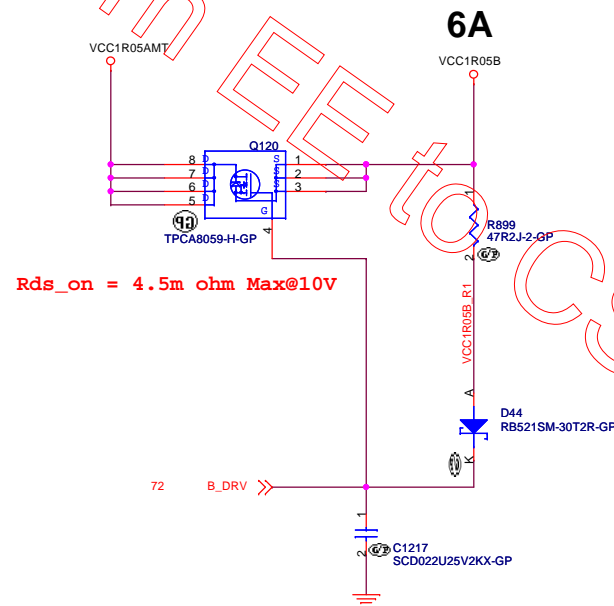
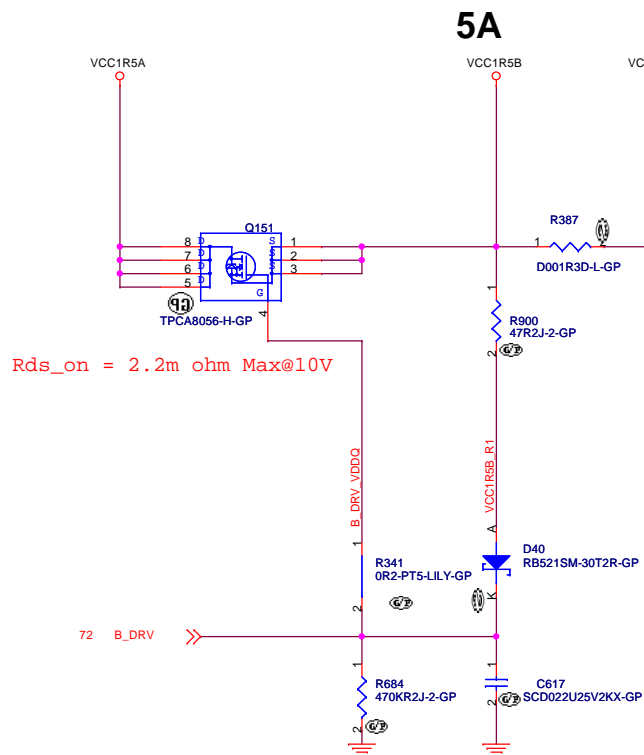
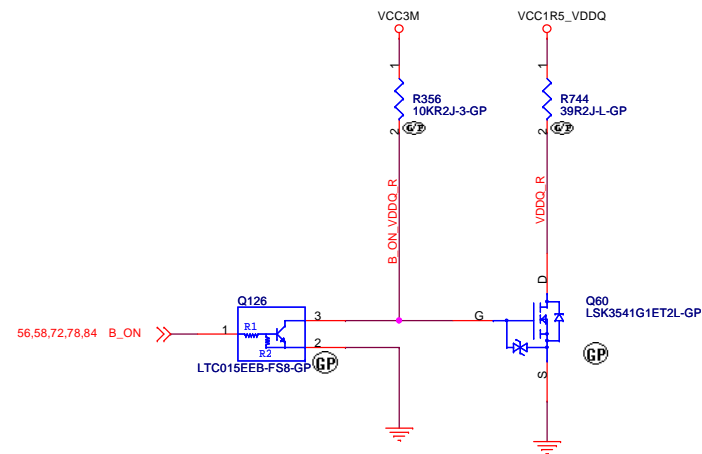
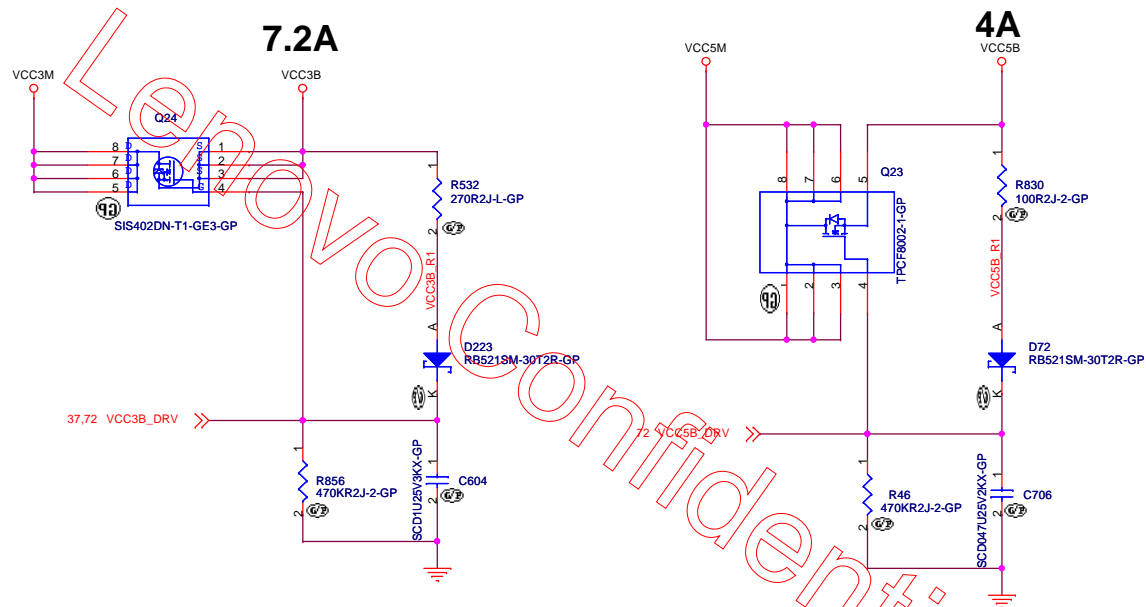
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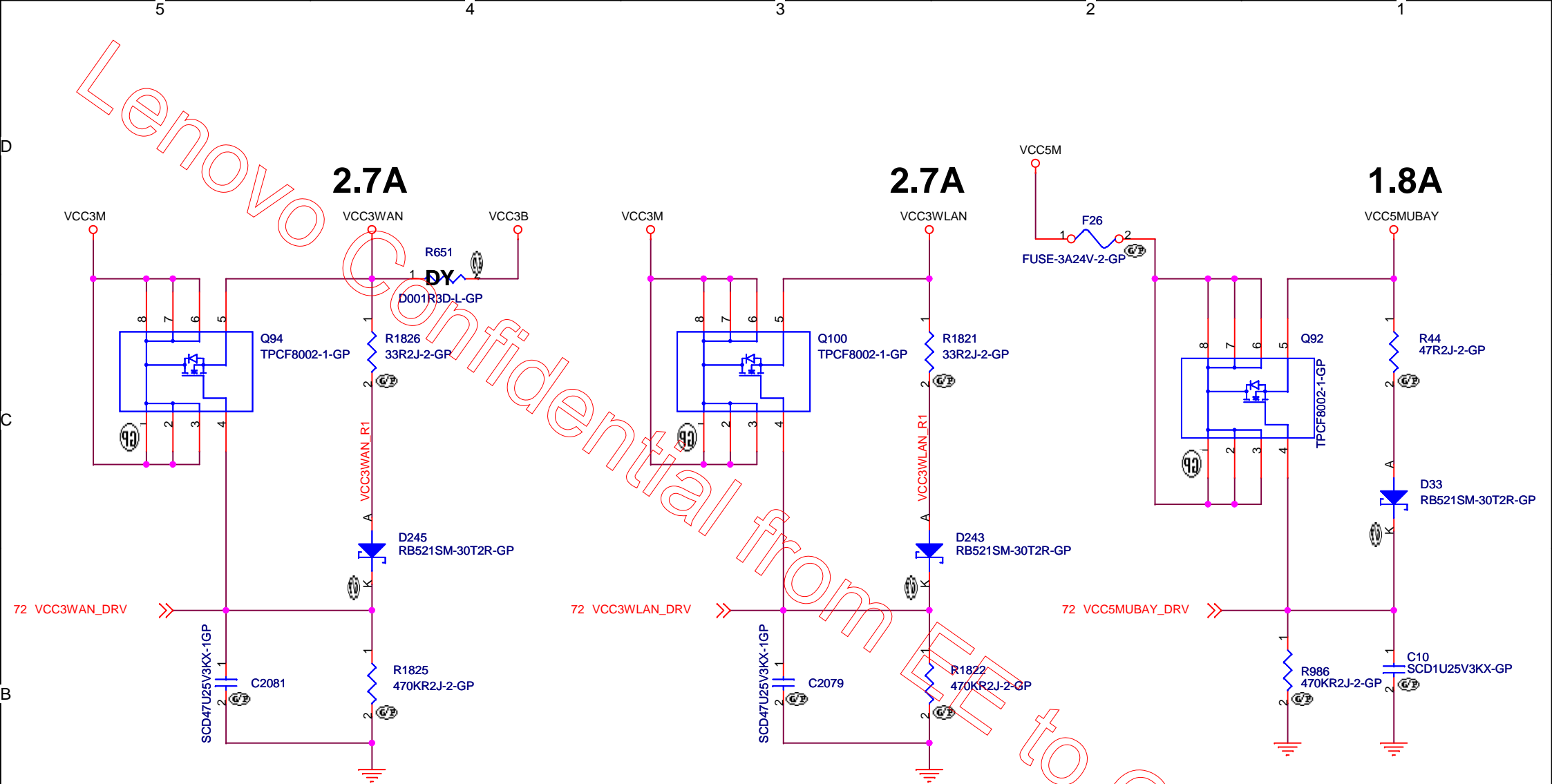
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A4

Document Number

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Rev
-1

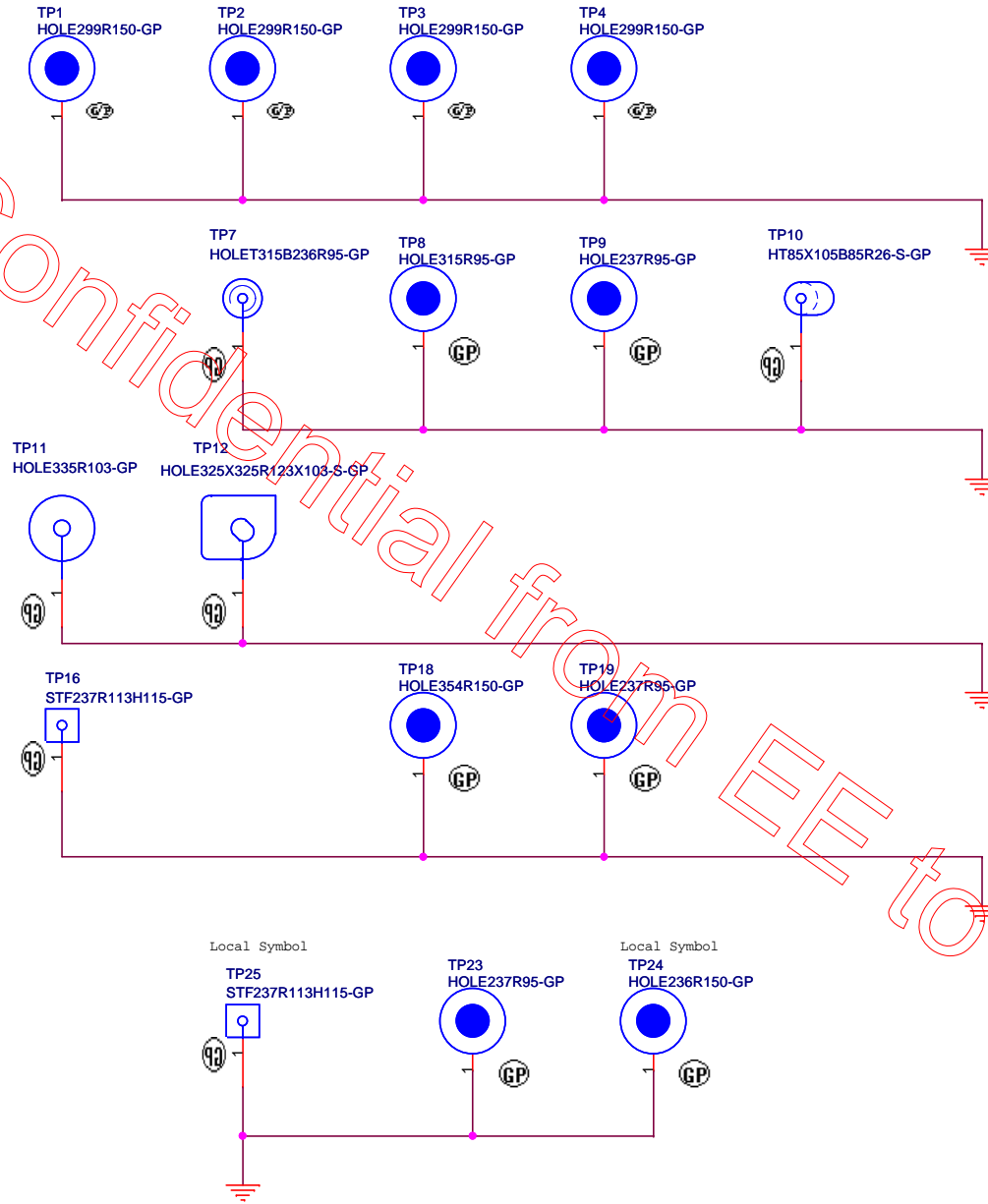
Date: Monday, March 12, 2012

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PTH FOR SCREW HOLE



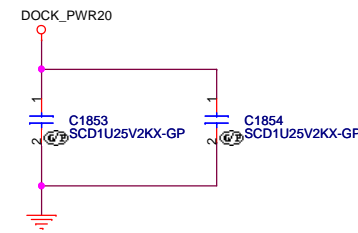
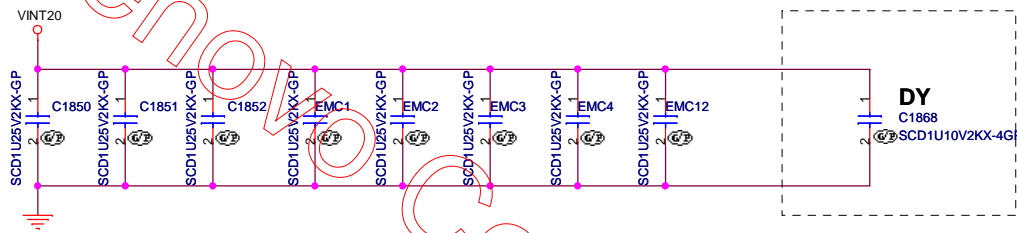
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		21F, 88, Sec. 1, Hsin Tai-Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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HOLES/GND/PADS			
Size	Document Number		Rev
Custom	SHINAI-4 UMA		-1
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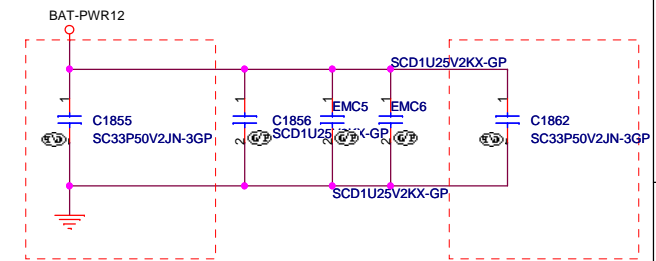
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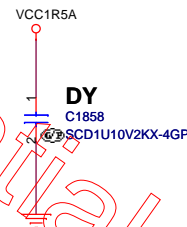
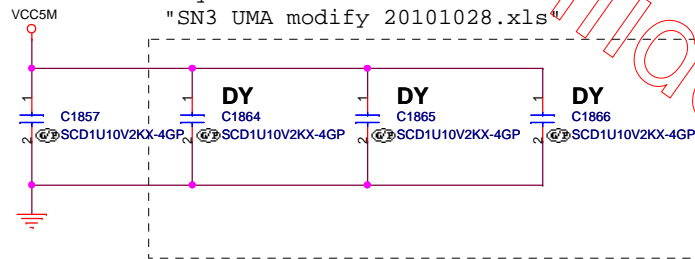
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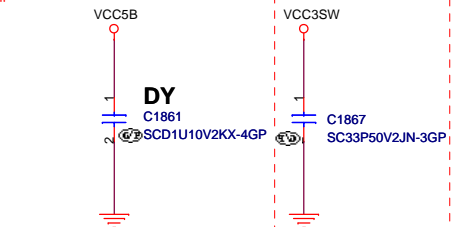
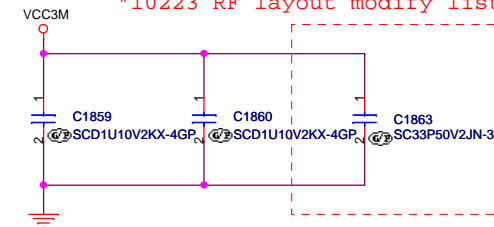
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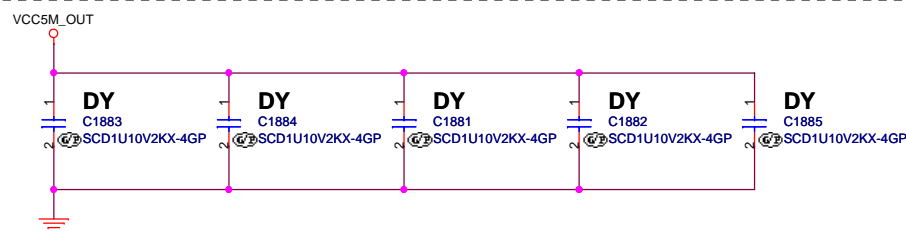
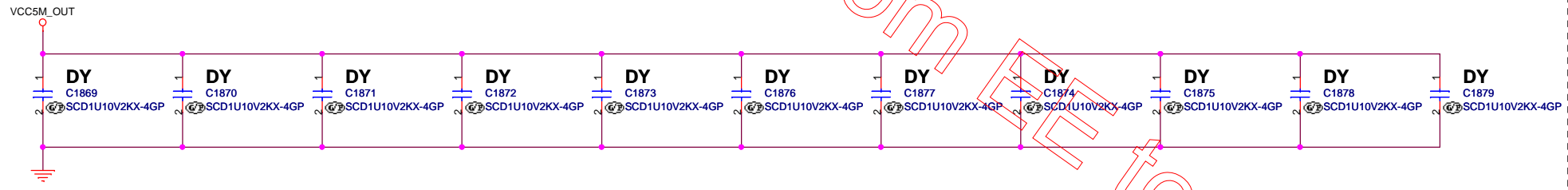
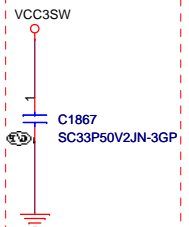
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1103.xls"



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Taipei Hsien 221, Taiwan, R.O.C.

Title		
EMI DECOUPLING		
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VT1318M Parameters For Sandy Bridge

Master IC		SV	ULV
U48		VT1318M	VT1318M
# of slave for CPU	2		1
Slave for CPU	U47	VT1324S	VT1324S
	U49	VT1324S	no stuff
Inductor for CPU	L28	BPW10040	no stuff
	L14	no stuff	MPCH0730LR12
# of slave for GPU		1	1
Slave for GPU	U50	VT1324S	VT1324S
Inductor for GPU	L29	MPCH0730LR12	MPCH0730LR12

		SV		ULV	
R_SEL[0]	pin 38	R1574	191	1.0%	249
R_SEL[1]	pin 37	R1575	215	1.0%	215
R_SEL[2]	pin 36	R1576	0	5.0%	0
R_SEL[3]	pin 35	R1577	191	1.0%	191
R_SEL[4]	pin 44	R1571	191	1.0%	191
R_SEL[5]	pin 32	R1579	374	1.0%	374
R_SEL[6]	pin 48	R1567	37.4	1.0%	37.4
R_REF	pin 34	R1578	20K	0.5%	20K
ROSC	pin 39	R1572	75K	1.0%	75K

			SV		ULV	
LL_R1_CPU	pin 15 - pin 16	R1599	10K	0.5%	10K	0.5%
LL_R2_CPU	pin 16 - pin 17	R1600	17.4K	0.5%	9.09K	0.5%
	pin 16 - pin 17	R1601	0	5.0%	0	5.0%
LL_C1_CPU	pin 15 - pin 16	C1086	22pF		22pF	
LL_C2_CPU	pin 16 - pin 17	C1087	22pF		22pF	
LL_RLEAD_CPU	pin 15 - pin 16	R1595	13K	1.0%	10K	1.0%
LL_CLEAD_CPU	pin 15 - pin 16	C1091	1000pF		1000pF	
LL_RLAG_CPU	pin 16 - pin 17	R1596	no stuff		no stuff	
LL_CLAG_CPU	pin 16 - pin 17	C1092	no stuff		no stuff	
RDES_CPU	pin 17 - pin 18	R1592	665	0.5%	536	0.5%
RINT_CPU	pin 18 - pin 19	R1593	665	1.0%	2.21K	1.0%
CINT_CPU	pin 18 - pin 19	C1088	10nF		10nF	
RPH11	IPH1_1 - pin 18	R1594	1.02K	1.0%	750	1.0%
RPH12	IPH1_2 - pin 18	R1598	1.02K	1.0%	no stuff	1.0%
IPHF11_R	pin 11	R1582	1.96K	1.0%	1.96K	1.0%
IPHF11_C	pin 11	C1076	10pF		10pF	
IPHF12_R	pin 10	R1581	1.96K	1.0%	no stuff	1.0%
IPHF12_C	pin 10	C1075	10pF		no stuff	
R_MRAMP1	pin 12	R1584	16.2K	1.0%	20K	
R_MRAMP1_PU	pin 12	R1587	no stuff		no stuff	1.0%
R_PWM2	Pin 6	R4	no stuff		0	5.0%
LL_R1_GPU	pin 24 - pin 23	R1069	10K	0.5%	10K	0.5%
LL_R2_GPU	pin 23 - pin 22	R1610	8.25K	0.5%	8.25K	0.5%
	pin 23 - pin 22	R1611	0	5.0%	0	5.0%
LL_C1_GPU	pin 24 - pin 23	C1094	22pF		22pF	
LL_C2_GPU	pin 23 - pin 22	C1095	22pF		22pF	
LL_RLEAD_GPU	pin 24 - pin 23	R1606	30K	1.0%	30K	1.0%
LL_CLEAD_GPU	pin 24 - pin 23	C1097	1000pF		1000pF	
LL_RLAG_GPU	pin 23 - pin 22	R1607	no stuff		no stuff	
LL_CLAG_GPU	pin 23 - pin 22	C1098	no stuff		no stuff	
RDES_GPU	pin 22 - pin 21	R1604	665	0.5%	665	0.5%
RINT_GPU	pin 21 - pin 20	R1605	3.24K	1.0%	3.24K	1.0%
CINT_GPU	pin 21 - pin 20	C1096	10nF		10nF	
RPH21	IPH2_1 - pin 21	R1608	1K	1.0%	1K	1.0%
IPHF21_R	pin 28	R1580	1.96K	1.0%	1.96K	1.0%
IPHF21_C	pin 28	C1077	no stuff		no stuff	
R_MRAMP2	pin 27	R1586	15.4K	1.0%	15.4K	1.0%
R_MRAMP2_PU	pin 27	R1590	56.2K	1.0%	56.2K	1.0%

			SV	ULV
		C1090	4.7uF	no stuff
		R1589	10 1.0%	no stuff
		C1089	0.1uF	no stuff
		C1082	0.22uF	no stuff
		C1083	1uF	no stuff
		C1080	1uF	no stuff
		C1084	10uF	no stuff
		C1079	10uF	no stuff
		C1081	10uF	no stuff
		C1085	10uF	no stuff
		L50	MPZ1608S300A	no stuff
		L51	MPZ1608S300A	no stuff
		C1087	2200pF	no stuff

Vcore Coutput

	SV			ULV	
C669	22uF	2125	22uF	2125	
C670	22uF	2125	22uF	2125	
C671	22uF	2125	22uF	2125	
C672	22uF	2125	22uF	2125	
C673	22uF	2125	22uF	2125	
C674	22uF	2125	22uF	2125	
C675	22uF	2125	22uF	2125	
C676	22uF	2125	22uF	2125	
C677	22uF	2125	22uF	2125	
C678	22uF	2125	22uF	2125	
C679	22uF	2125	22uF	2125	
C680	22uF	2125	22uF	2125	
C681	22uF	2125	22uF	2125	
C682	22uF	2125	22uF	2125	
C683	22uF	2125	22uF	2125	
C684	22uF	2125	22uF	2125	
C685	22uF	2125	22uF	2125	
C686	22uF	2125	22uF	2125	
C687	22uF	2125	22uF	2125	
C688	22uF	2125	22uF	2125	
C689	22uF	2125	22uF	2125	
C690	22uF	2125	22uF	2125	
C691	22uF	2125	22uF	2125	
C692	22uF	2125	22uF	2125	
C693	22uF	2125	22uF	2125	
C694	22uF	2125	22uF	2125	
C695	22uF	1608	22uF	1608	
C696	22uF	1608	22uF	1608	
C697	22uF	1608	N/A	1608	
C698	22uF	1608	N/A	1608	
C750	22uF	2125	N/A	2125	
C1109	22uF	2125	N/A	2125	
C1110	N/A	1608	N/A	1608	
C1111	N/A	1608	N/A	1608	
C1112	N/A	1608	N/A	1608	
C1113	N/A	1608	N/A	1608	

GFX Coutput

	SV			ULV	
C642	22uF	2125	22uF	2125	
C643	22uF	2125	22uF	2125	
C644	22uF	2125	22uF	2125	
C645	22uF	2125	22uF	2125	
C646	22uF	2125	22uF	2125	
C647	22uF	2125	22uF	2125	
C648	22uF	2125	22uF	2125	
C649	22uF	2125	22uF	2125	
C650	22uF	2125	22uF	2125	
C651	22uF	2125	22uF	2126	
C652	22uF	2125	22uF	2125	
C663	22uF	2125	22uF	2125	
C664	22uF	2125	22uF	2125	
C665	22uF	2125	22uF	2125	
C666	22uF	2125	22uF	2125	
C667	22uF	2125	22uF	2125	
C1114	22uF	1608	22uF	1608	
C1115	22uF	1608	22uF	1608	
C1116	22uF	1608	22uF	1608	
C1117	22uF	1608	22uF	1608	
C1118	22uF	1608	22uF	1608	
C1119	22uF	1608	22uF	1608	
C1120	22uF	1608	22uF	1608	
C1121	22uF	1608	22uF	1608	

<Core Design>

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